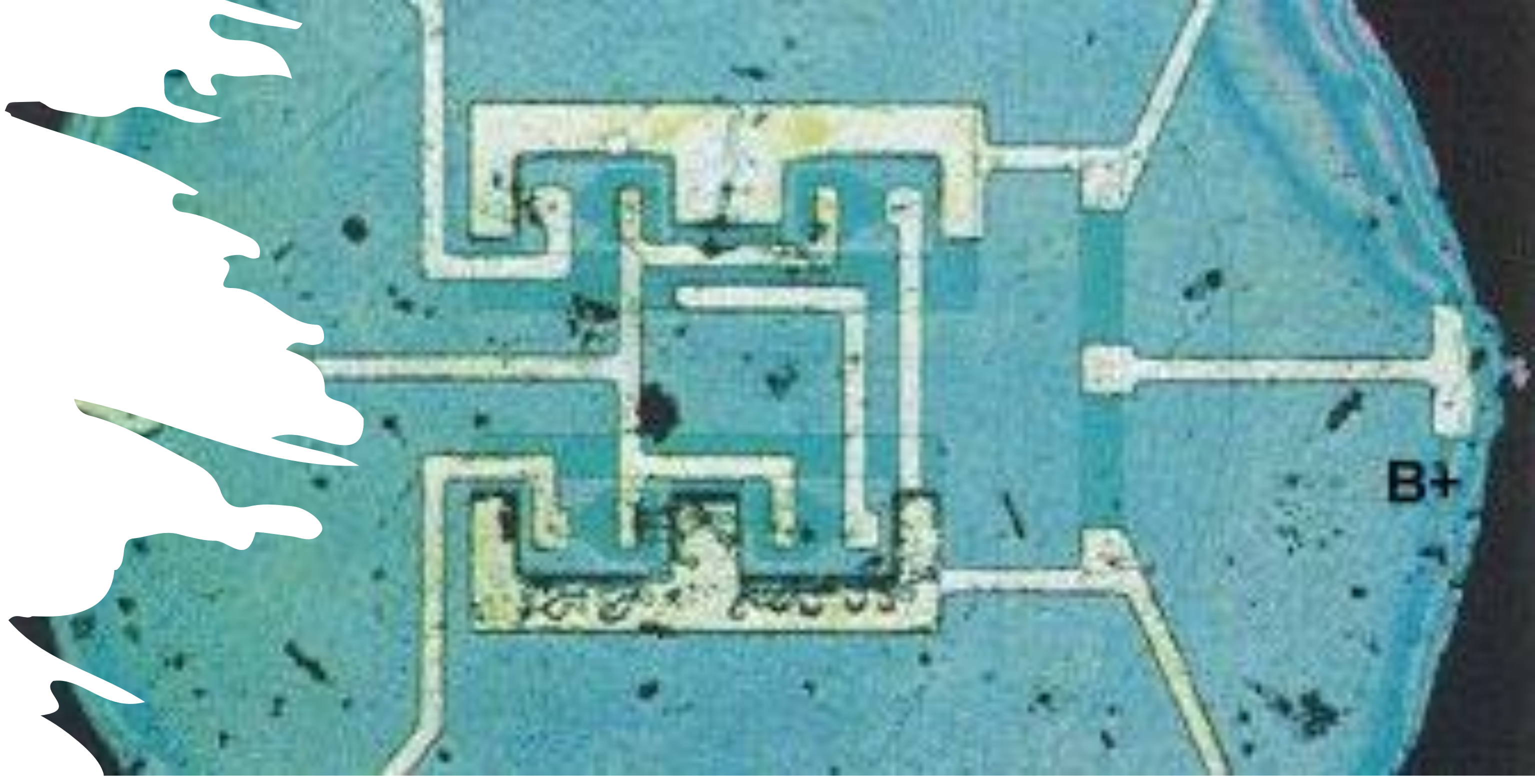
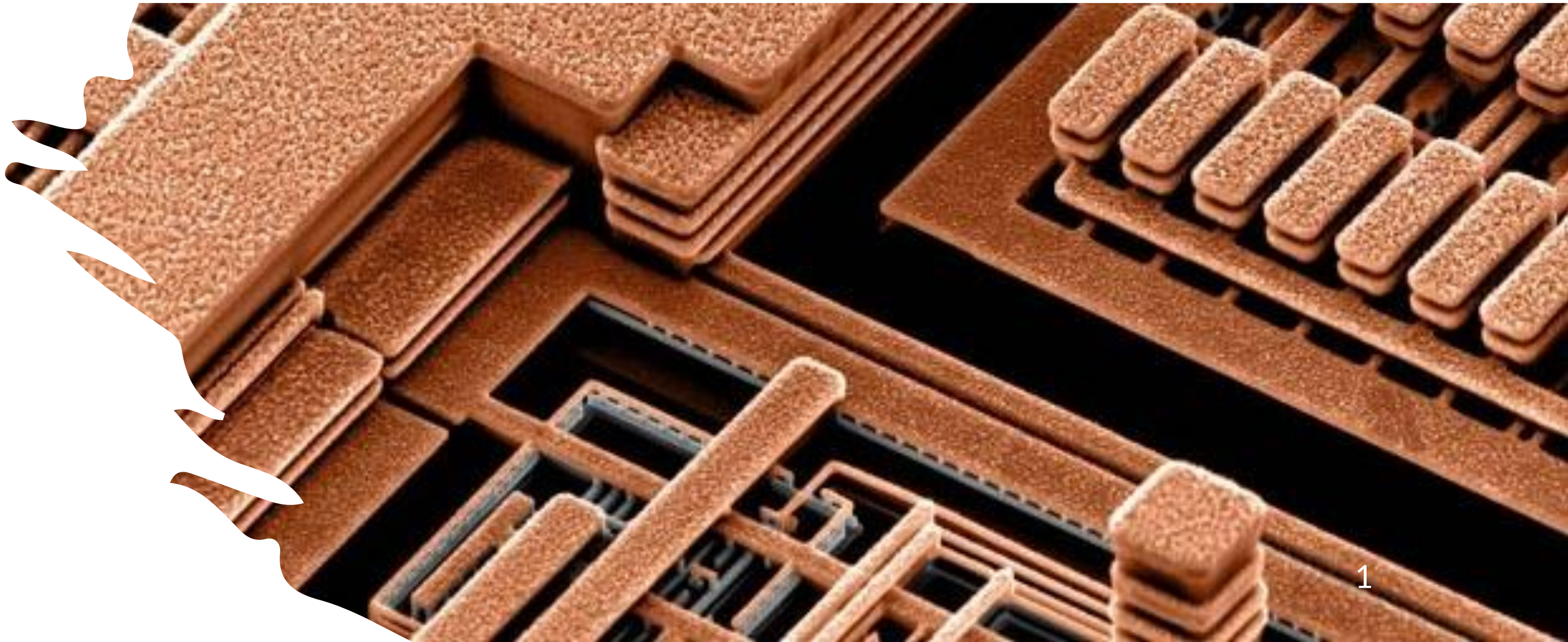
Advanced Interconnects

- 1959: The monolithic IC, Robert Noyce @ Fairchild, with **Al** metal lines

- 1997: the first **Cu** interconnects in microprocessors @ IBM

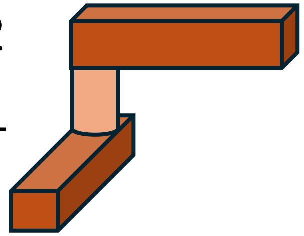
→Better than Cu





Yuan Tu,
AtomSolve Corp.

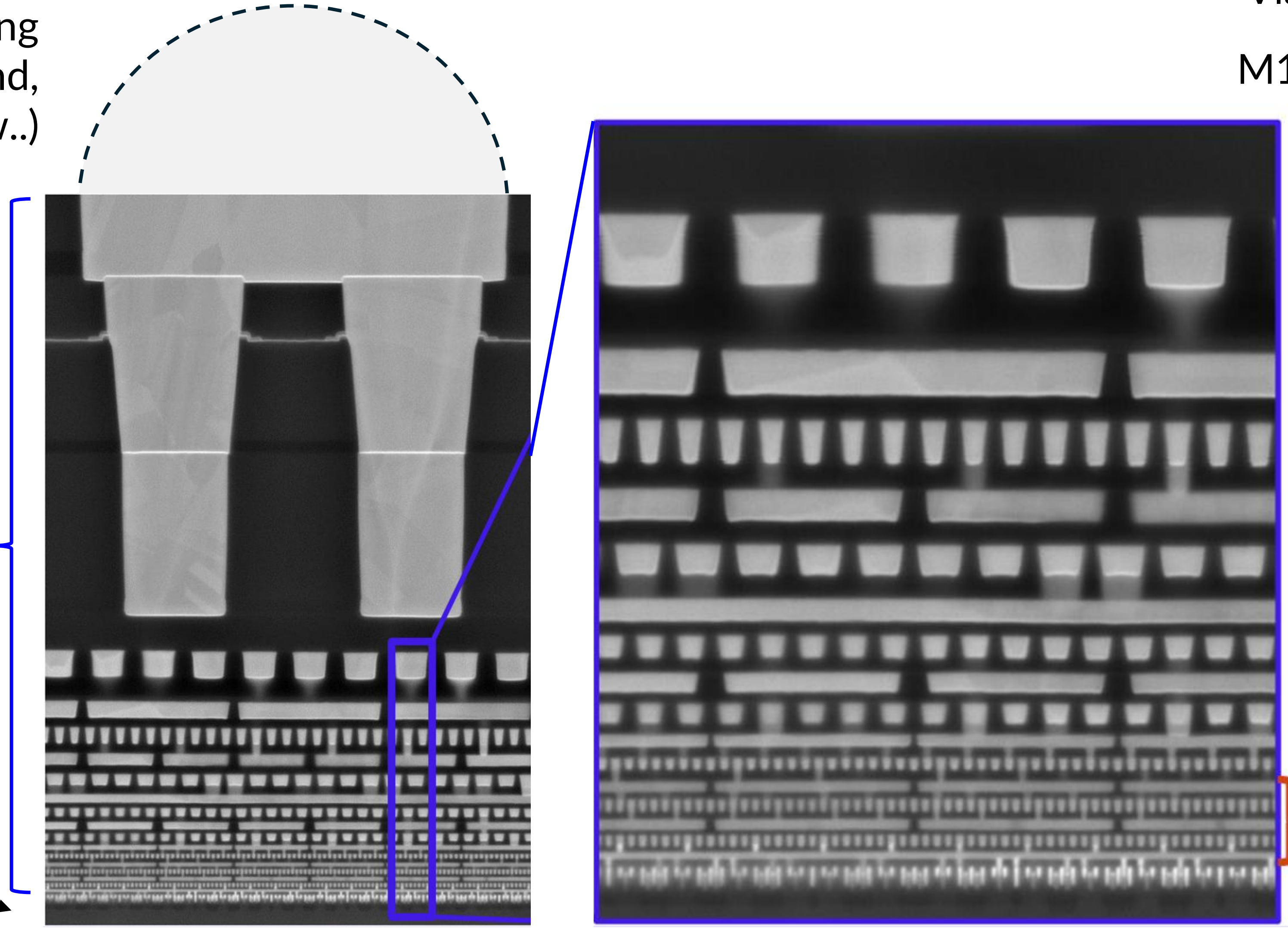
BEOL: on-chip interconnect (e.g. INTEL 4, 18 layers)



Advanced Packaging (flip-chip, wire-bond, w2w..)

Back-end-of-line (BEOL) Interconnects

Front-end-of line (FEOL) Transistors

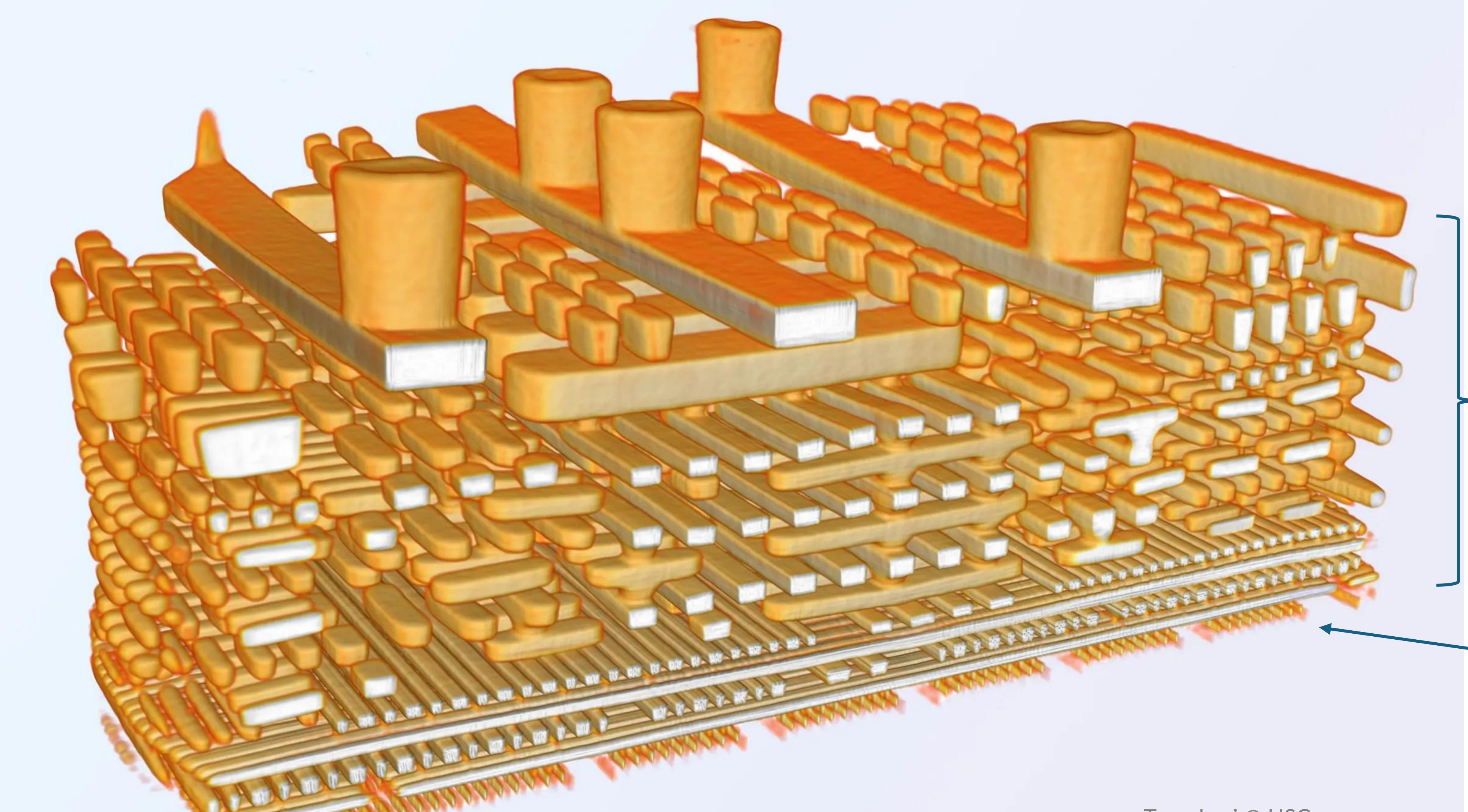


Most critical local interconnects

https://www.semiconductor-digest.com/intel-4-process-drops-cobalt-interconnect-goes-with-tried-and-tested-copper-with-cobalt-liner-cap/

AMD Ryzen 5 processor (TSMC 7nm node)

3D view by X-ray imaging



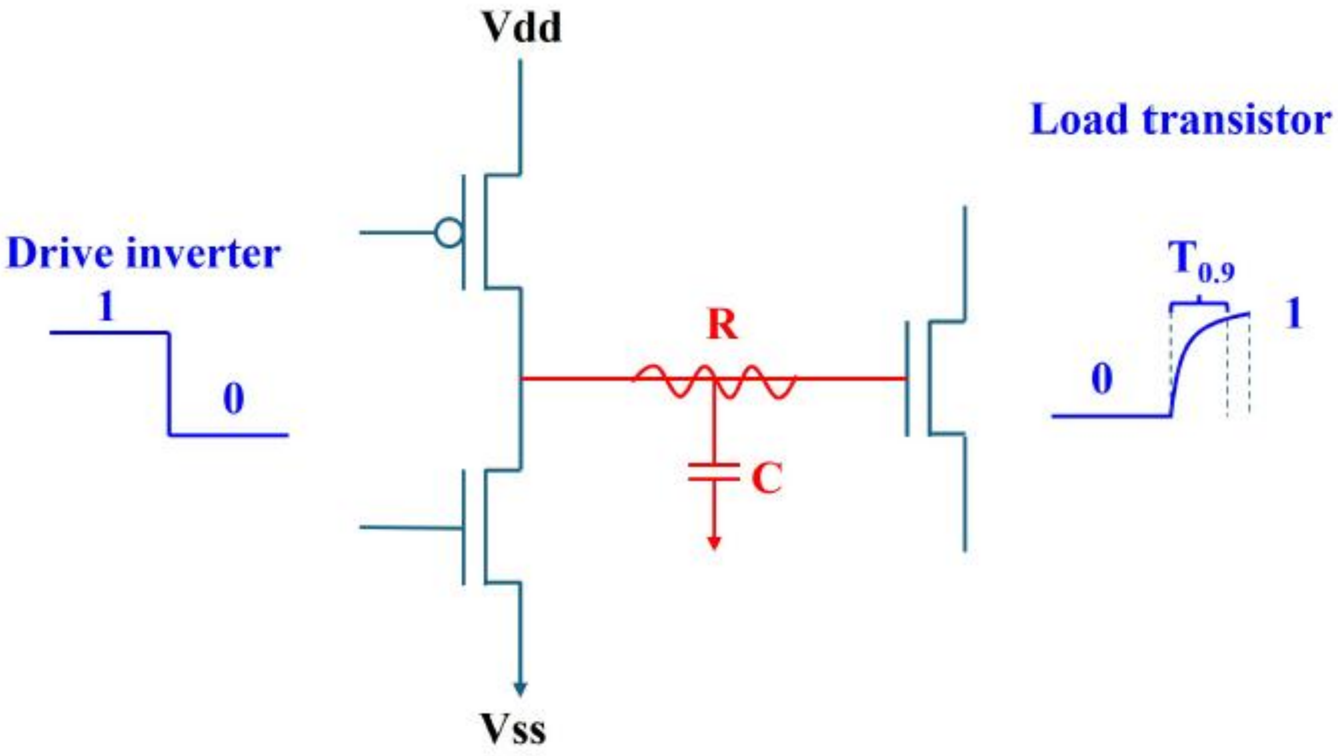
interconnects

transistors

ptychographic X-ray laminography,
resolution: 4nm

Tony Levi @ USC
Gabriel Aeppli @ ETH Zürich

RC delay



信號延遲：

$$\tau = RC$$

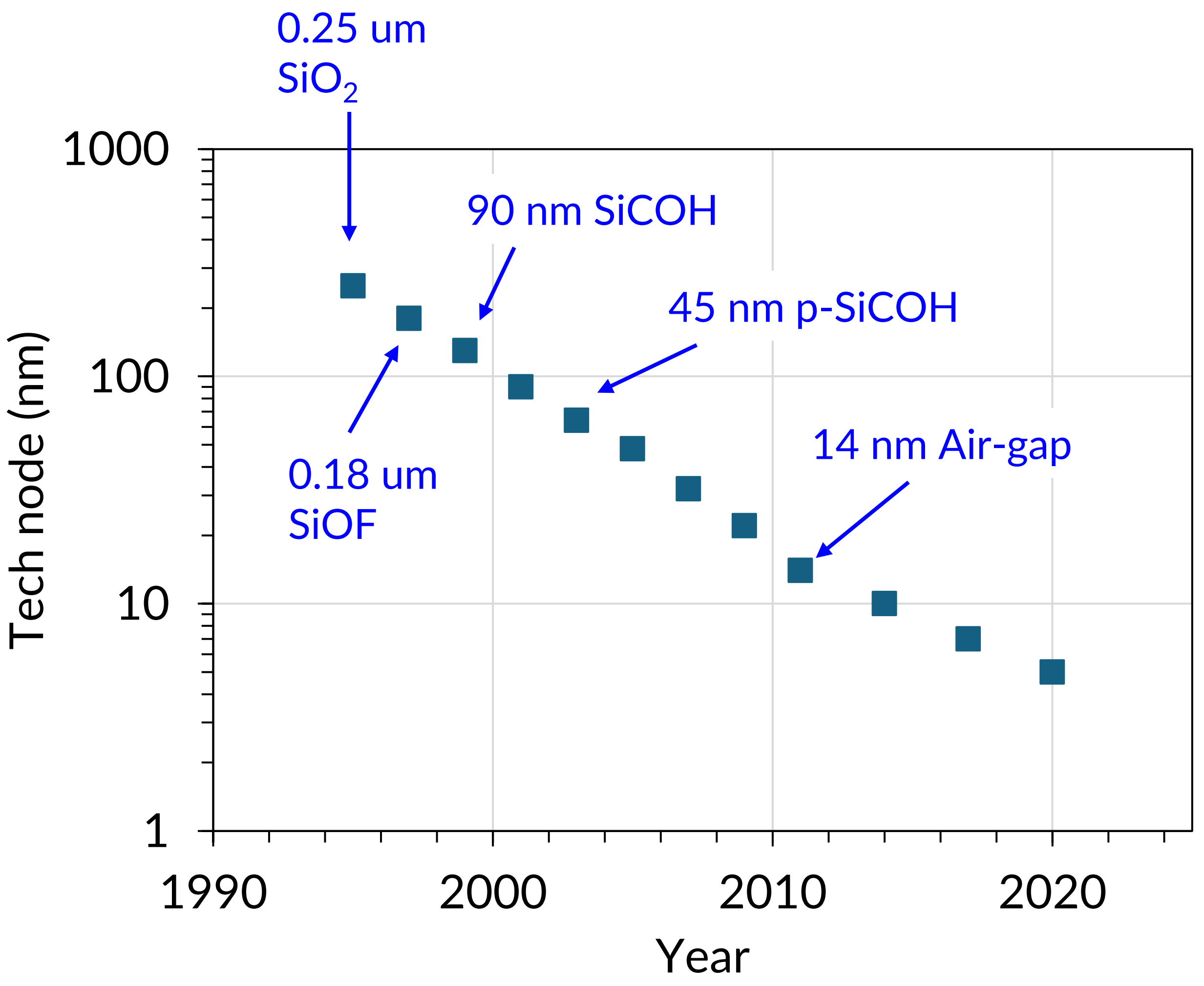
Material	Ag	Cu	Au	Al	W
ρ ($\mu\Omega$·cm)	1.587	**1.678**	2.214	**2.65**	5.28
T_m (°C)	961	**1084**	1064	**660**	3422

- Metal line $R = \boldsymbol{\rho}\frac{L}{WT}$
- Dielectric $C = \boldsymbol{k}\frac{LT}{S}$

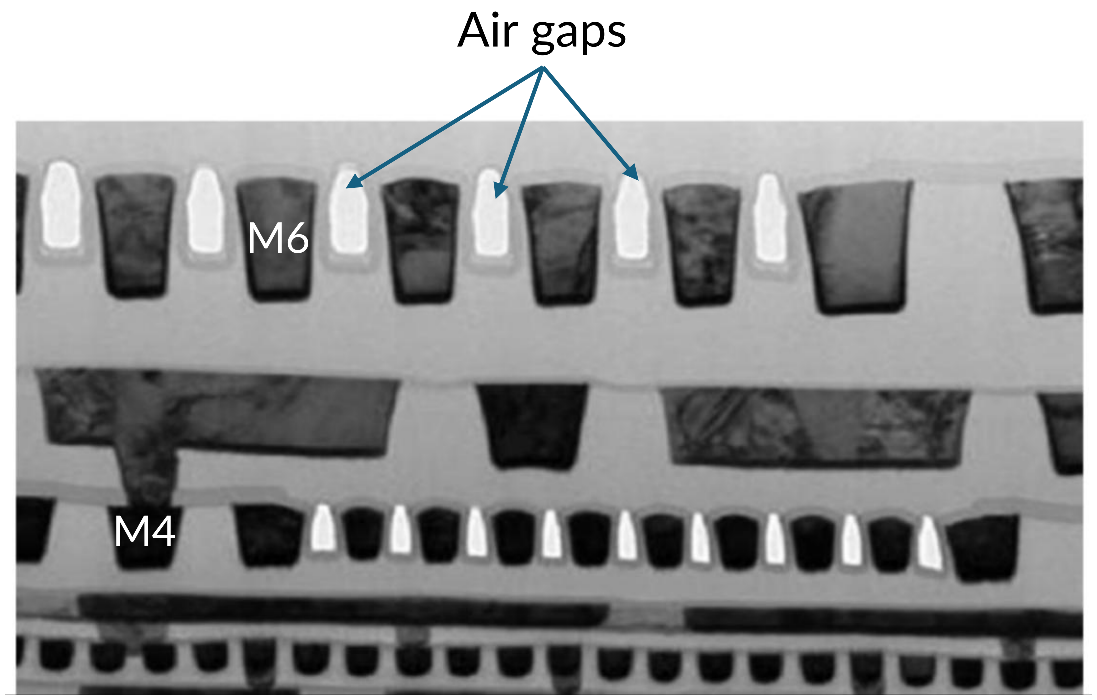
Material	SiN	SiCN	SiO_2	SiOF	SiCOH	Air
κ	6.8 ~ 7.3	4.0 ~ 5.0	**4.0**	3.5 ~ 3.8	2.2 ~ 3.2	1.0

Low-k

Dielectrics at tech nodes



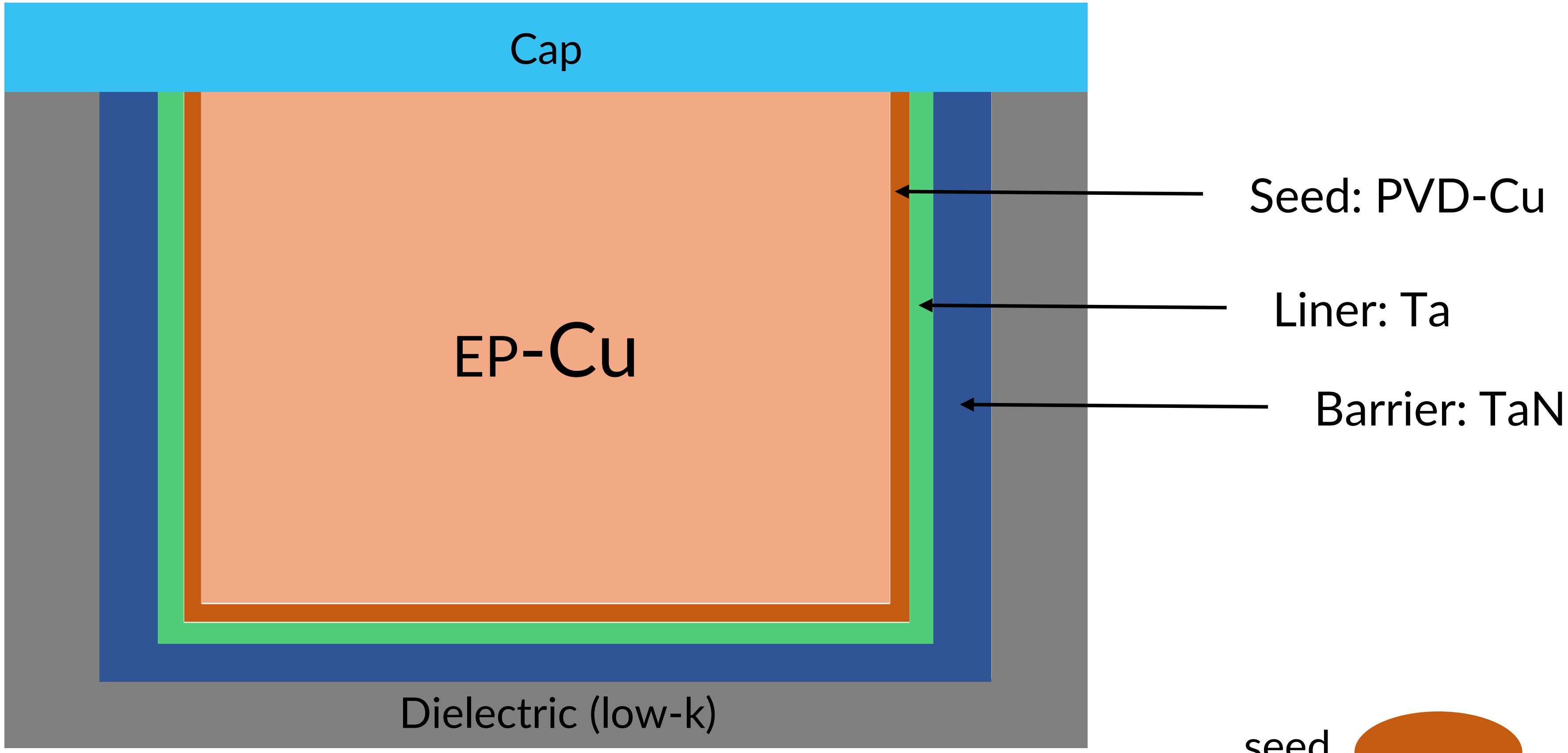
Jeff Gambino (ONSEMI), PROCESS TECHNOLOGY FOR COPPER INTERCONNECTS

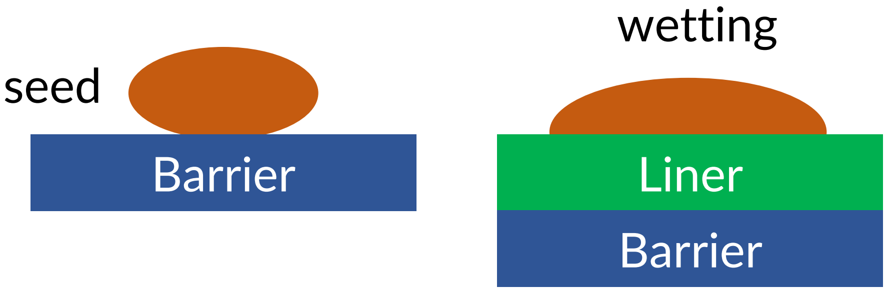


Intel 14 nm

Fischer et al. (Intel), IEEE IITC 2015

Structure of Cu interconnect

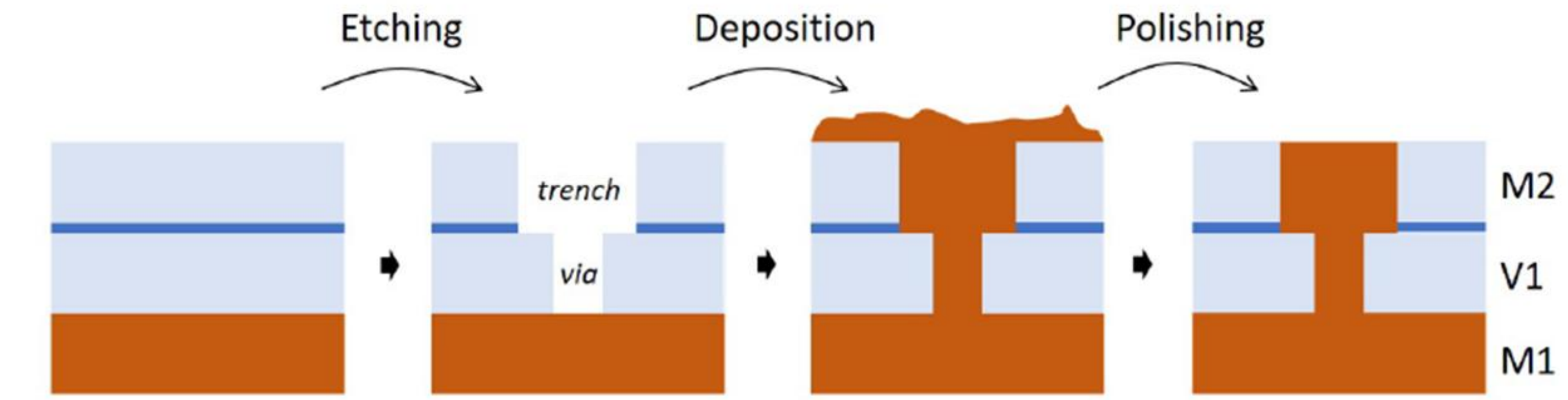




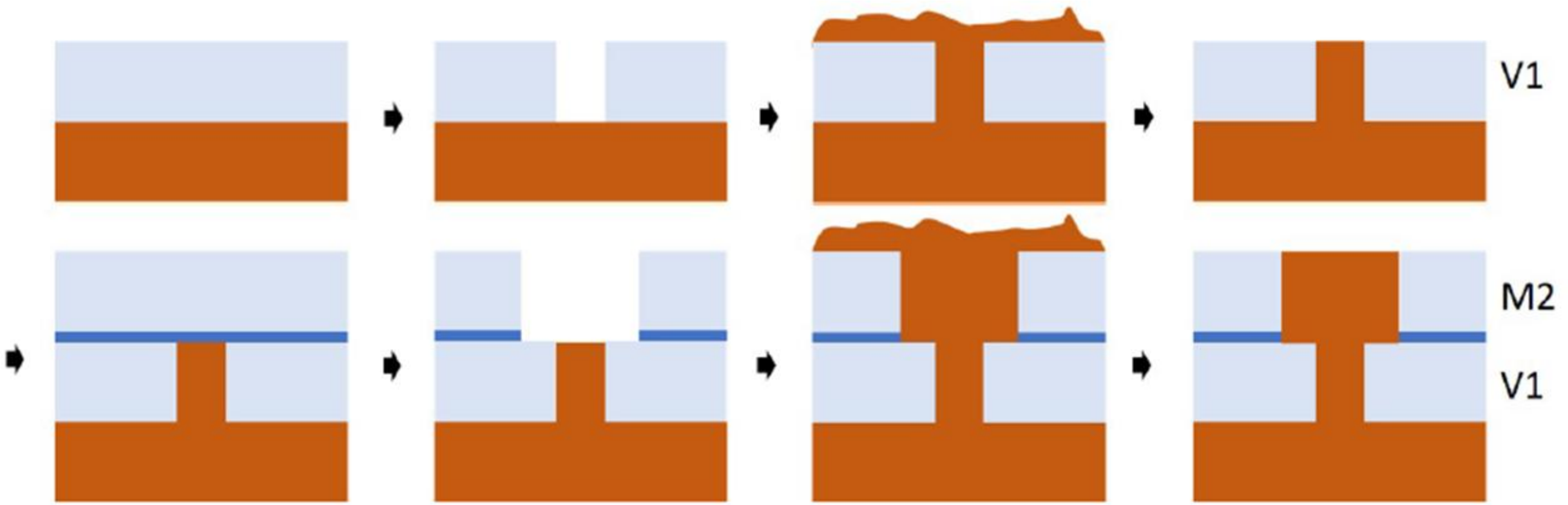
Yuan Tu,
AtomSolve Corp.

Damascene process

- Dual-damascene: Fill via and trench in once, V1 and M2 are the same material.

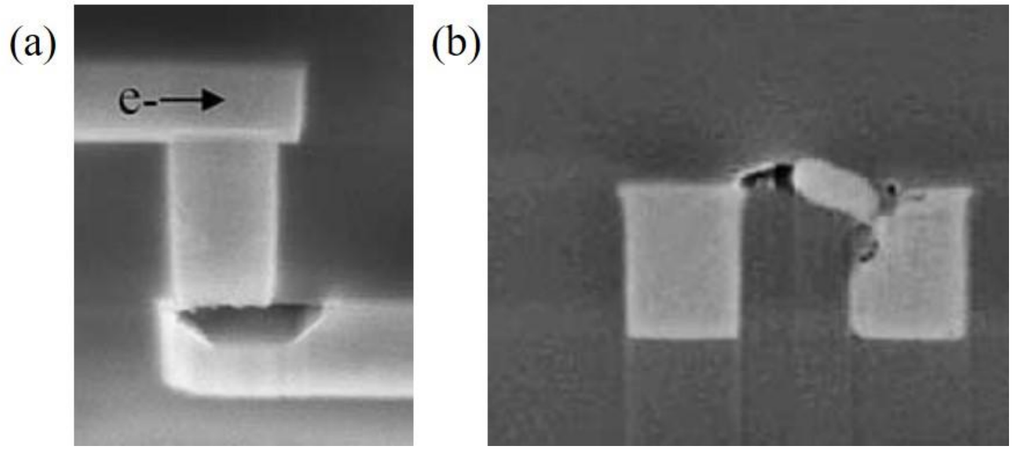


- Single-damascene: Fill via, polish, then fill trench. V1 and M2 can be different materials.



Reliability issues

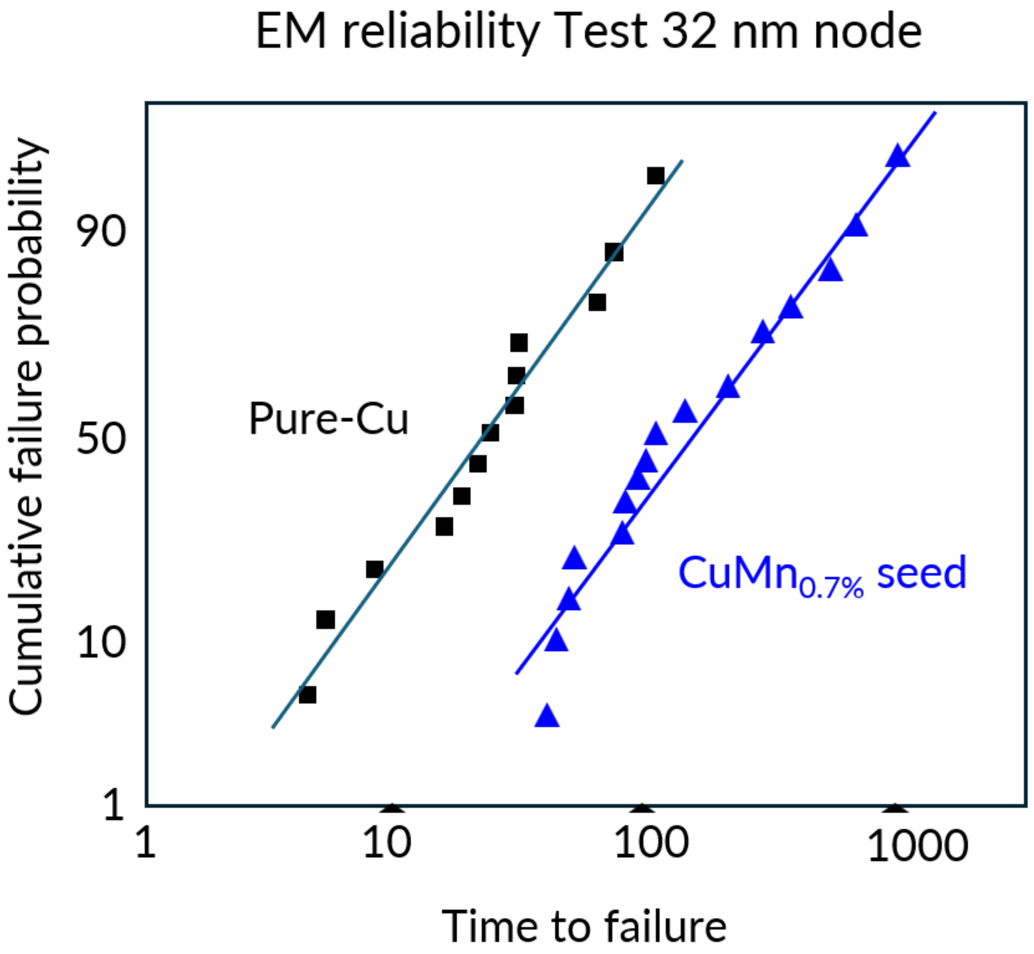
(1) Electro-migration (EM)



Ref: Hau-Riege, C. S., Microelectronics Reliability 44, 195–205 (2004).

(2) Stress-induced voids (SIV)

(3) Time dependent dielectric breakdown



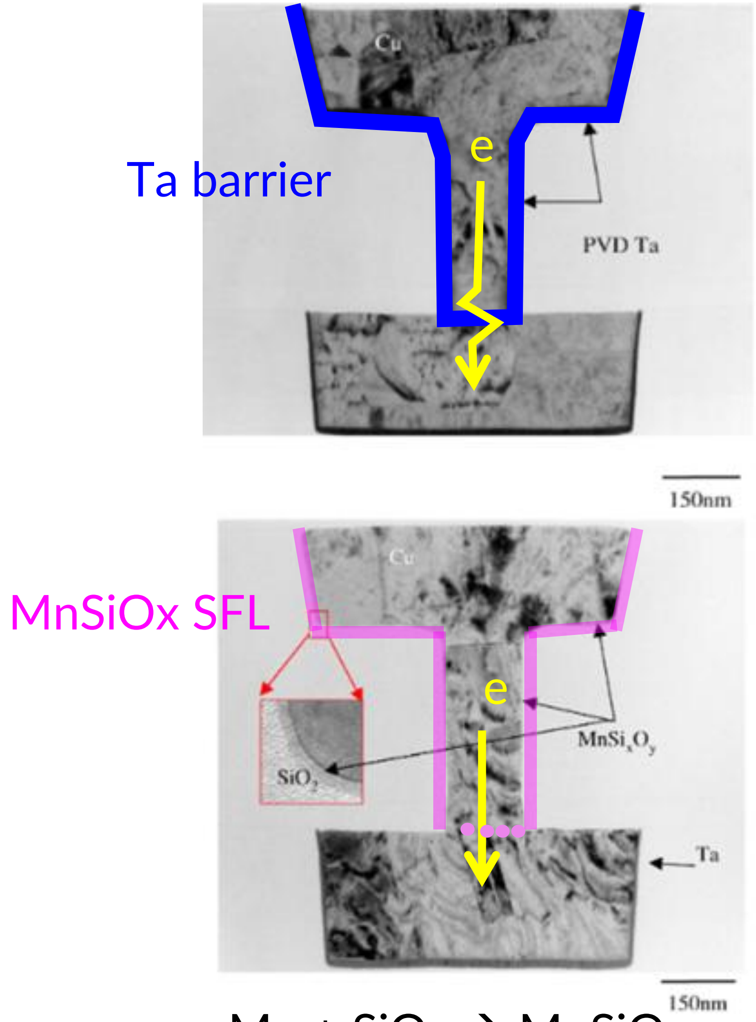
Nogami (IBM) et al., IEEE IEDM 2010

What's the role of Mn?

1. Koike et al., IEEE IITC pp.1648676 (2006);
2. Nogami et al., IEEE IEDM pp. 33.5.1-33.5.4 (2010)
3. Shimogaki et al., ECS J. Solid State Sci. Technol. 2 P471 (2013)

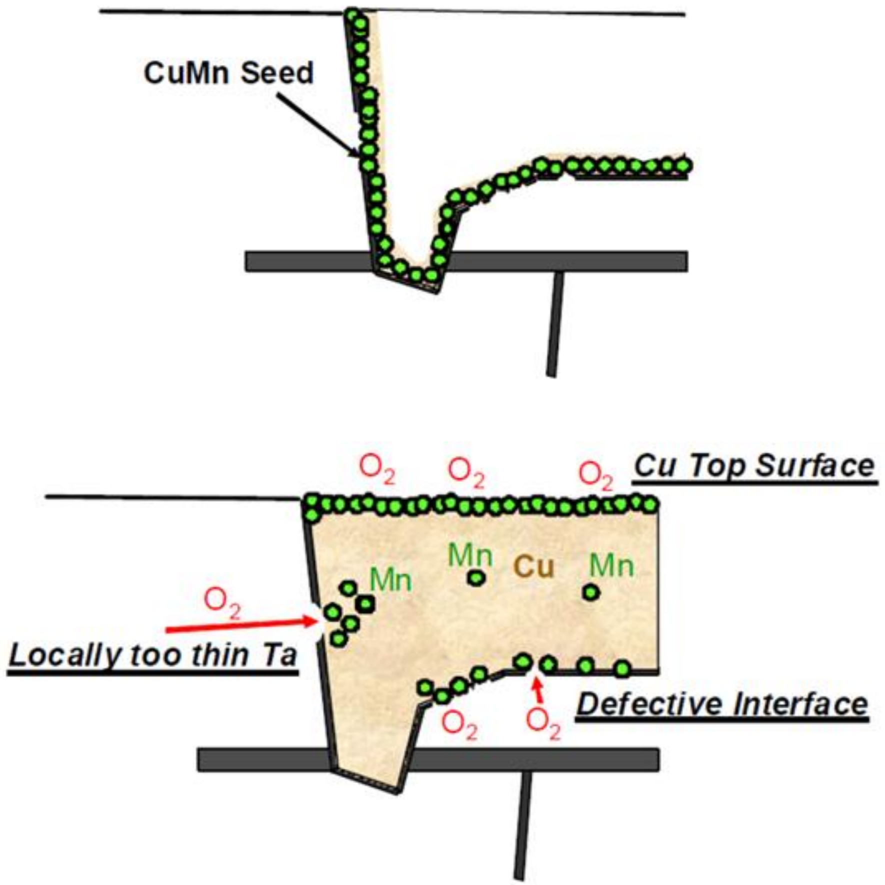
Role of Mn (1)

- **Self-forming layer**
  Prof. Koike (Tohoku)



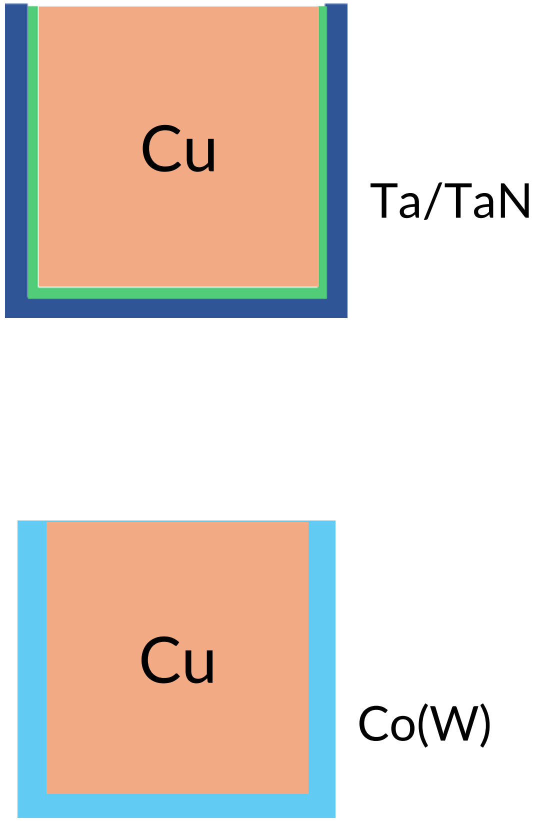
$Mn + SiO_2 \rightarrow MnSiOx$

- **"Scabbing model"**
  Dr. Nogami Takeshi (IBM)



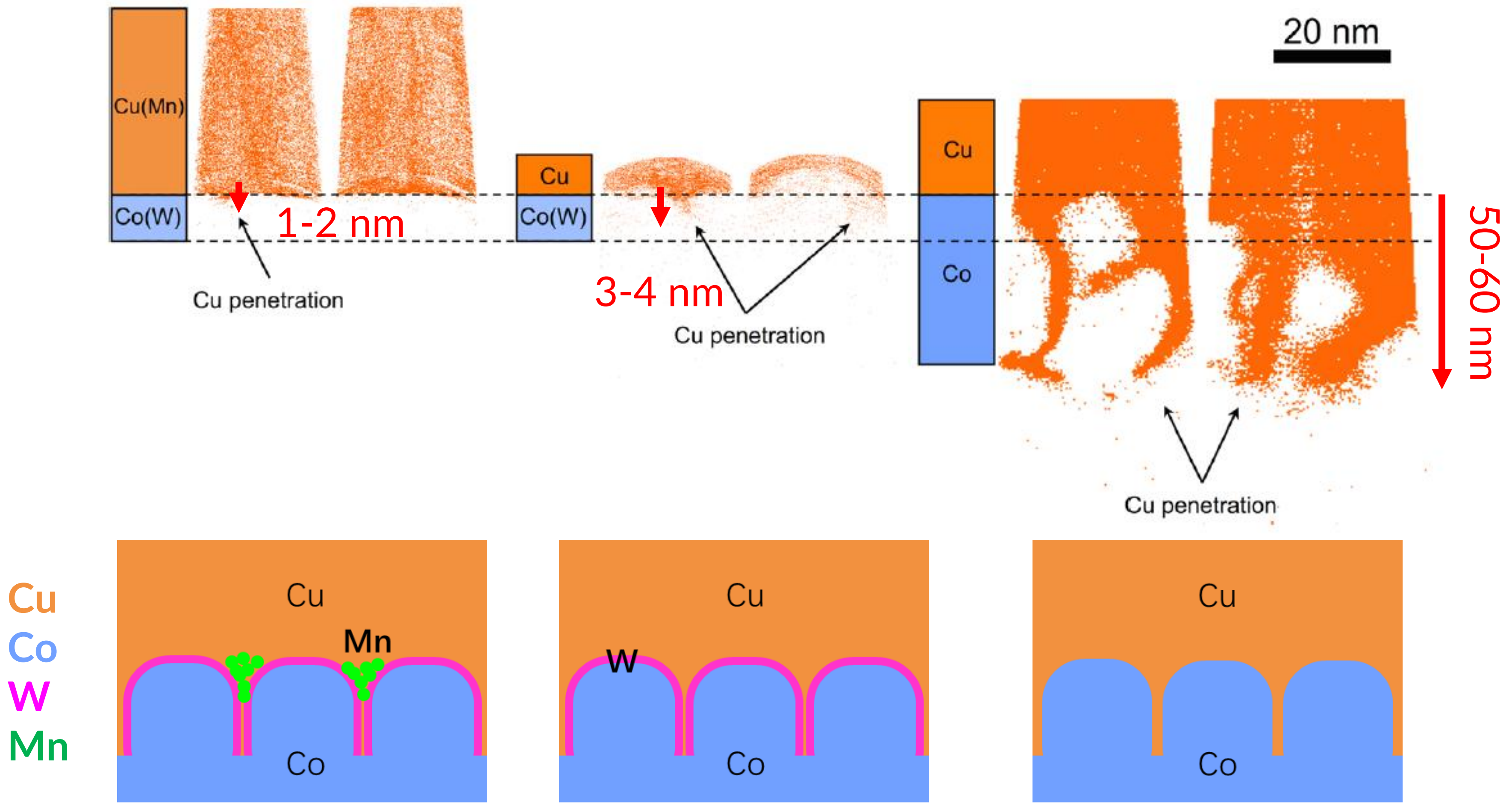
Mn compete with Cu for O, and fill voids

- **Co replace Ta/TaN**
  Prof. Shimogaki (UTokyo)



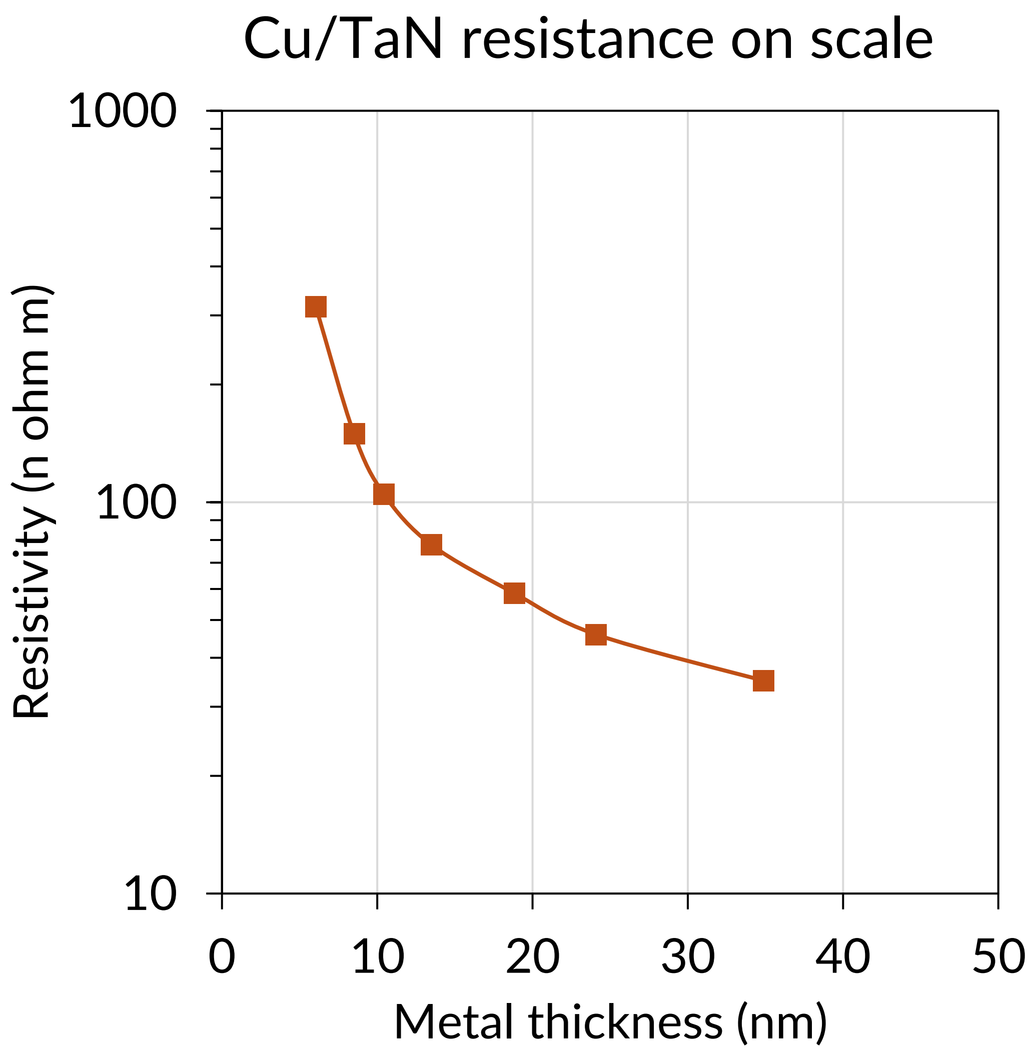
Role of Mn (2)

- Cu(Mn)/Co(W)
- Cu/Co(W)
- Cu/Co



Ref: Shima (UTokyo), Tu (Tohoku), Nagai et al., Role of W and Mn for reliable 1X nm ULSI Cu interconnects proved by APT (2014)

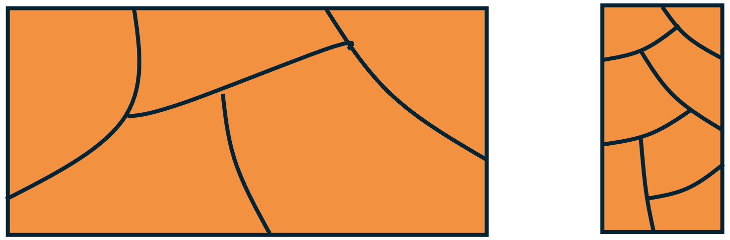
Cu Resistance increase with scaling



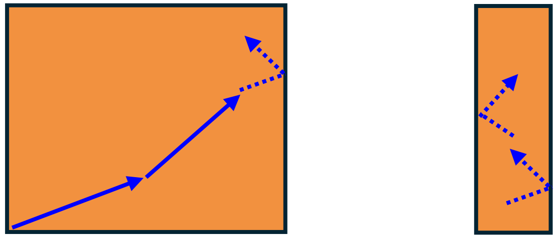
Data from IMEC: Materialia 24, 101511 (2022)

(1) Barrier ratio is increasing

(2) Grain boundary scattering

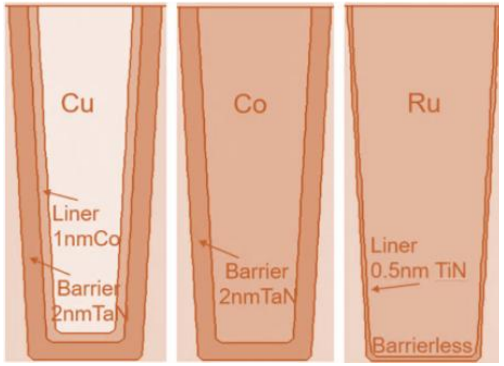


(3) Sidewall scattering (CD < Mean free path λ)

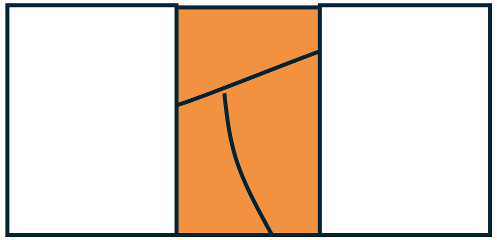


Regarding methods

(1) Barrier-less material, e.g. Ru



(2) Subtractive method



(3) Alternative materials: smaller λ

Metal	Cu	W	Mo	Co	Ni	Ru
λ_e (nm)	39.9	15.5	11.2	11.8	5.8	6.6

Gall, J. Appl. Phys. 119, 085101 (2016)

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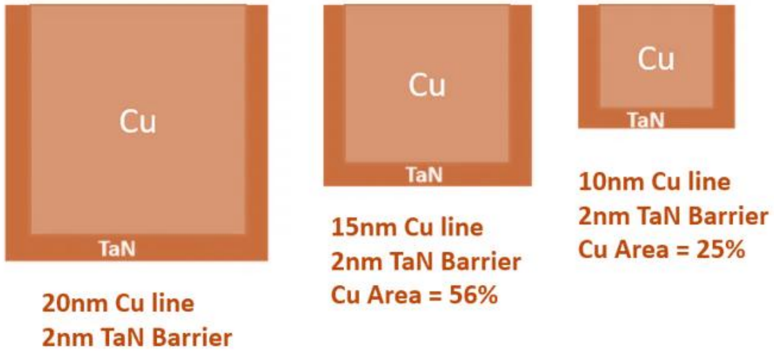

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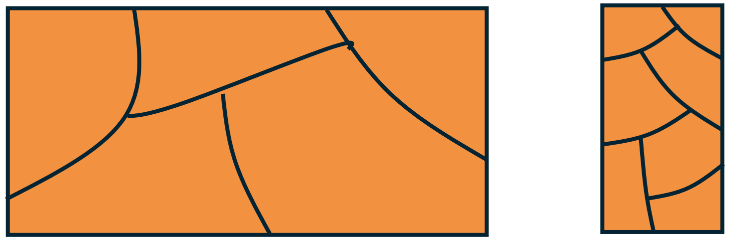

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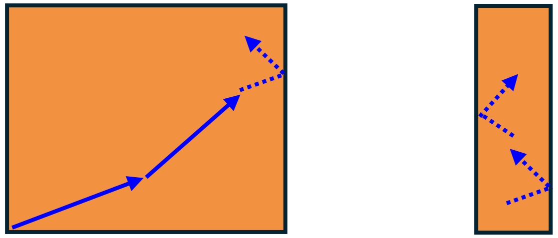

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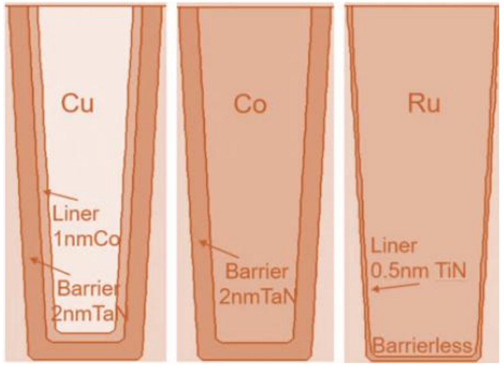

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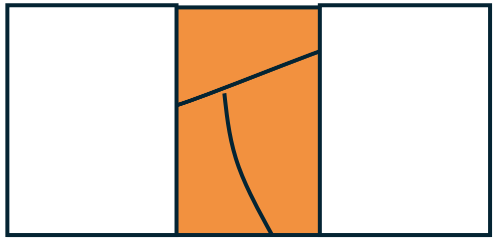

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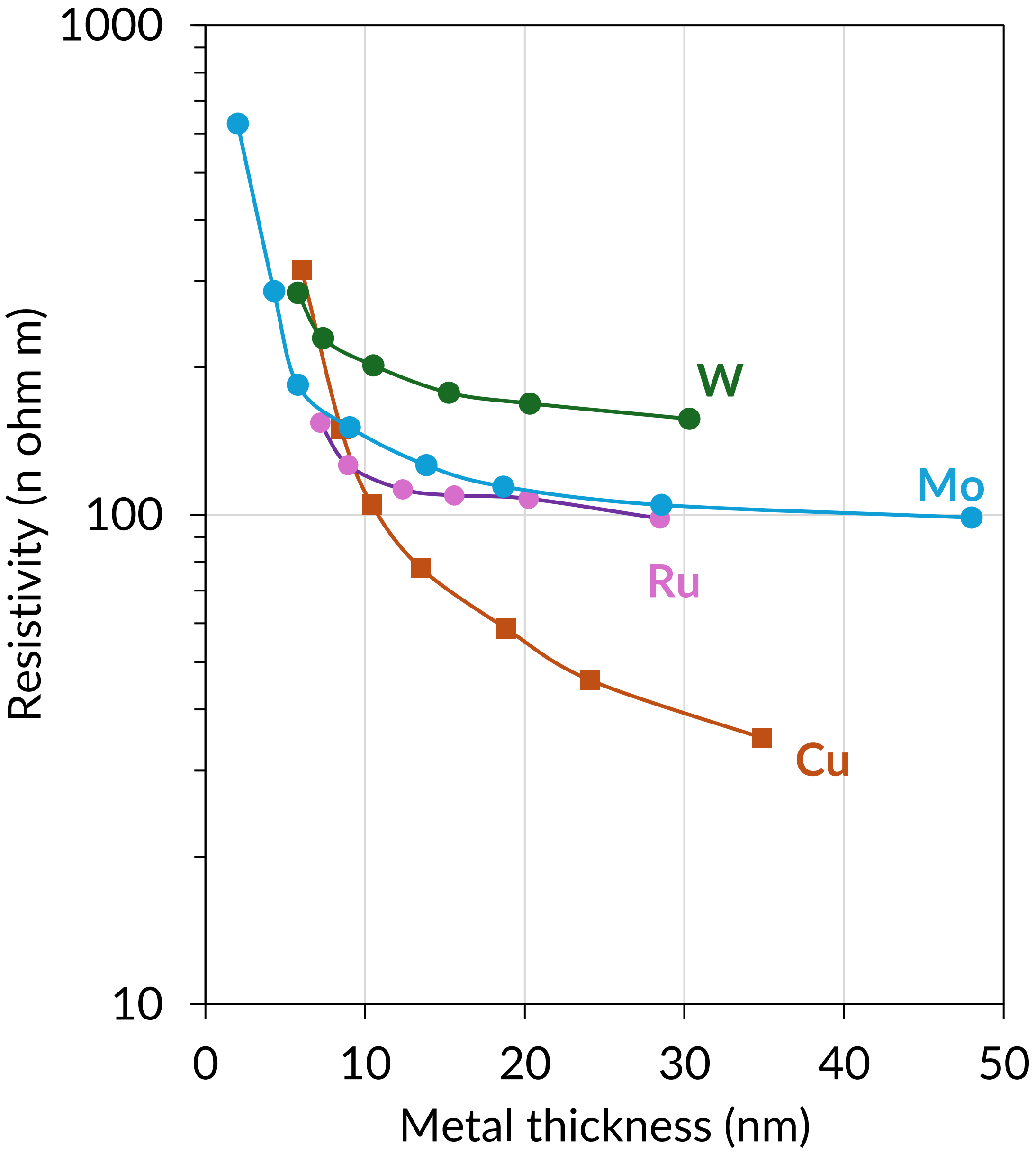
Gall, J. Appl. Phys. 119, 085101 (2016)

Data from IMEC: Materialia 24, 101511 (2022)



Yuan Tu,
AtomSolve Corp.

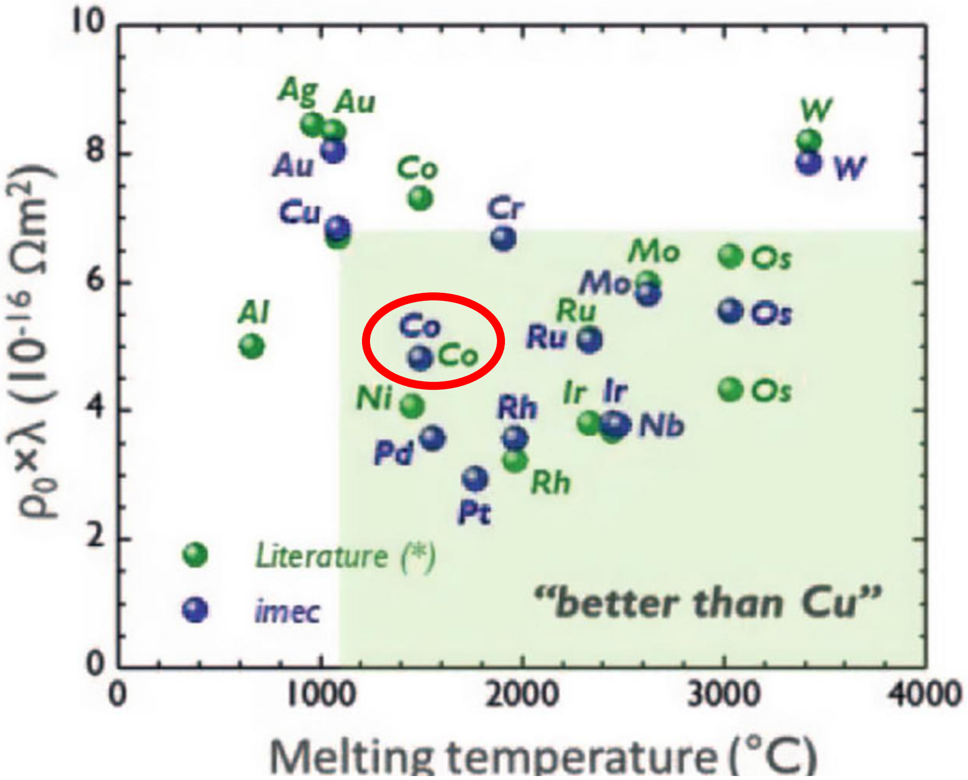
Better than Copper

Figure of merits:

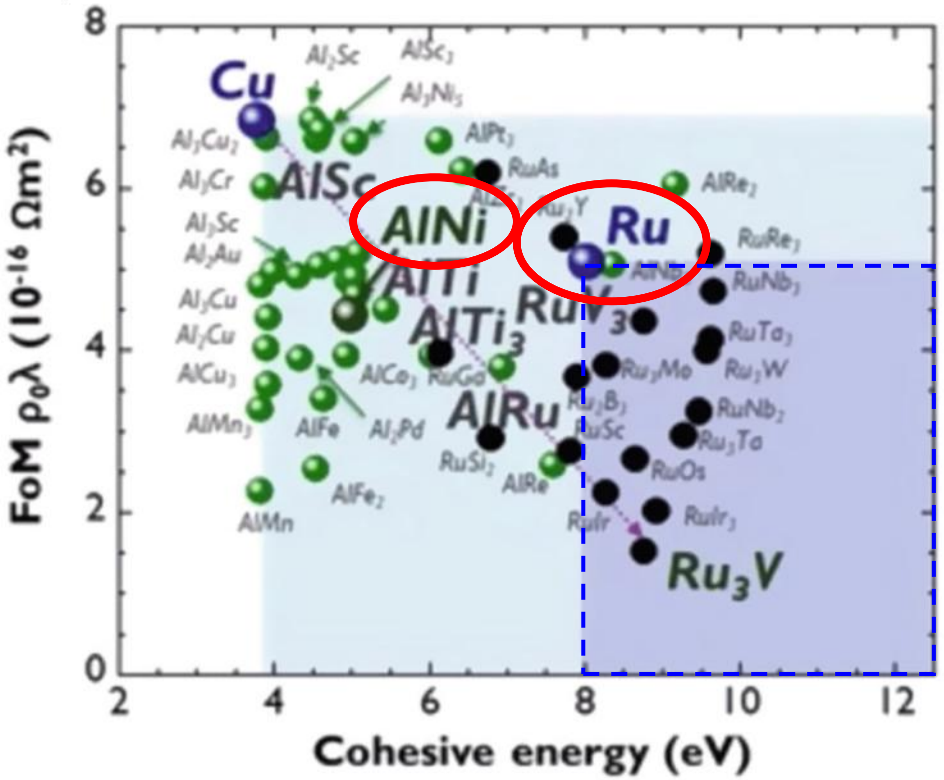
1. Lower resistivity at small scale → $\rho * \lambda$
2. Higher stability; → T_m, or cohesive energy

⇨

- Cobalt
- Ruthenium
- Nickel Aluminum (NiAl)



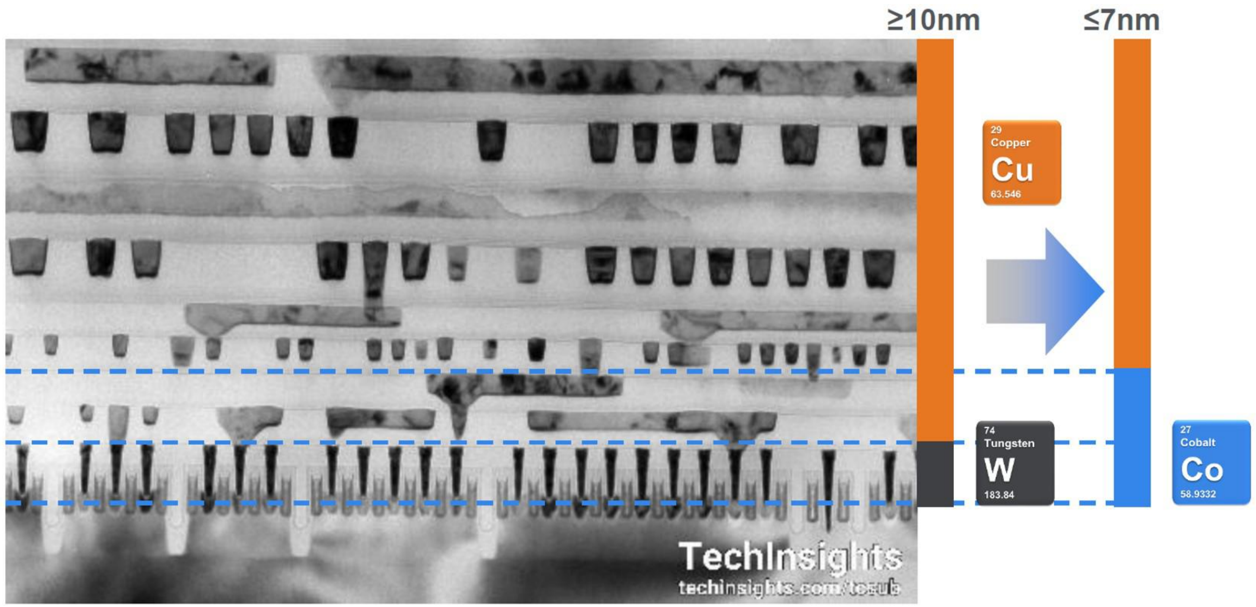
- **Elementary: Co, Ru, Mo, …**



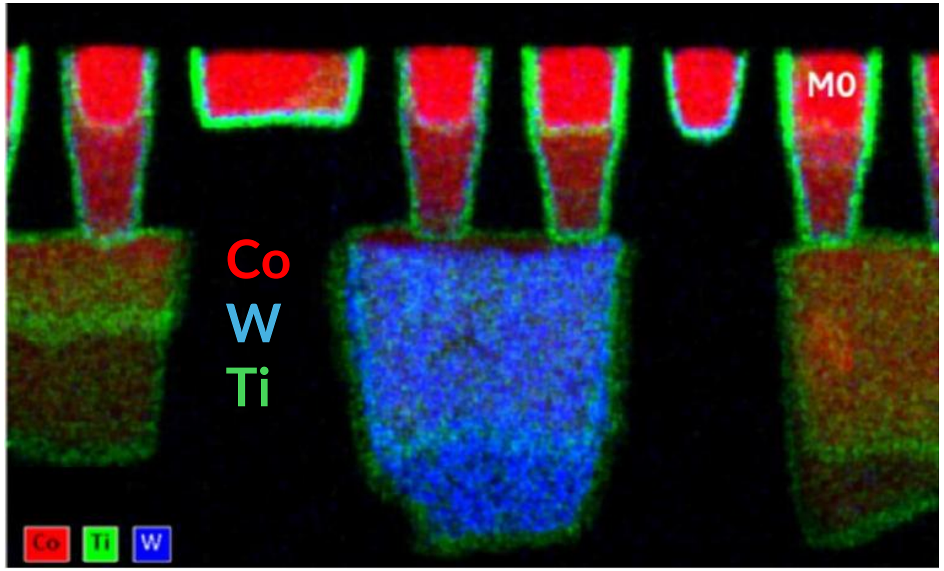
- **Binary IMCs: NiAl …**

Yuan Tu,
AtomSolve Corp.

Cobalt (1): AMAT (Contact, M0~M1), Intel (10nm: Contact & M0)



Courtesy of Techinsights



Griggio et al. IEEE IRPS 6E-3 (2018)

2018, Applied Materials:

- Co to replace W, and Cu

"Enabling the AI Era with New Materials: First Material Change in the Transistor Contact and Interconnect in 20 years."

Intel 10 nm

- Co used in Contact and M0.

Dual-damascene local interconnects featuring cobalt on 10 nm logic technology

Cobalt (2): Intel 4, Co→eCu

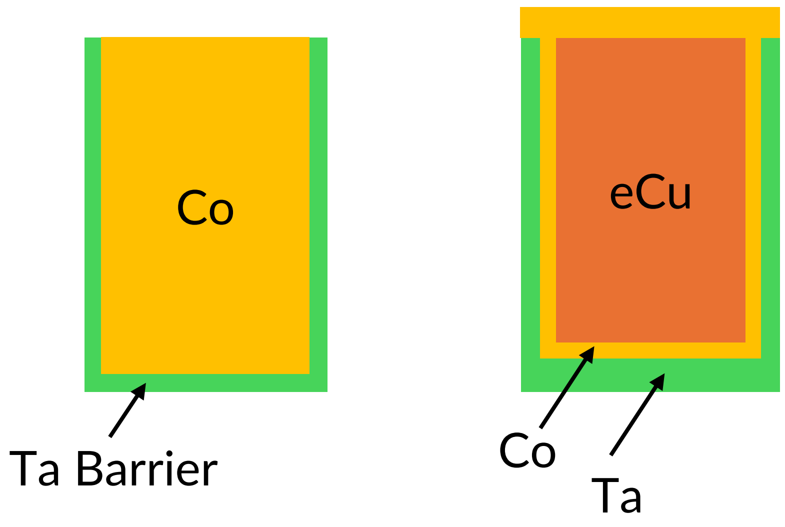
*eCu: Cu reflow

layer	Metal	Intel 7 Pitch(nm)
Fin	--	34
Contacted Gate	W/Co	54
M0	Co	40
M1	Co	36
M2	Cu	44
M3	Cu	52
M4	Cu	52
M5	Cu	84
M6	Cu	84
M7	Cu	84
M8	Cu	112
M9	Cu	112
M10	Cu	160
M11	Cu	160
M12	Cu	160
M13	Cu	160
M14	Cu	400
--	--	--
Thick M 0	Cu	1080
Thick M 1	Cu	11um

Layer	Metal	Intel 4 Pitch(nm)
Fin		30
Contacted Gate	W	50
M0	eCu	30
M1	eCu	50
M2	eCu	45
M3	eCu	50
M4	eCu	45
M5	Cu	60
M6	Cu	60
M7	Cu	84
M8	Cu	84
M9	Cu	98
M10	Cu	98
M11	Cu	130
M12	Cu	130
M13	Cu	160
M14	Cu	160
M15	Cu	280
GM0	Cu	1080
GM1	Cu	4000

Intel 7
Core: Co
Barrier: Ta

Intel 4
Core: eCu
Liner/Barrier: Co/Ta

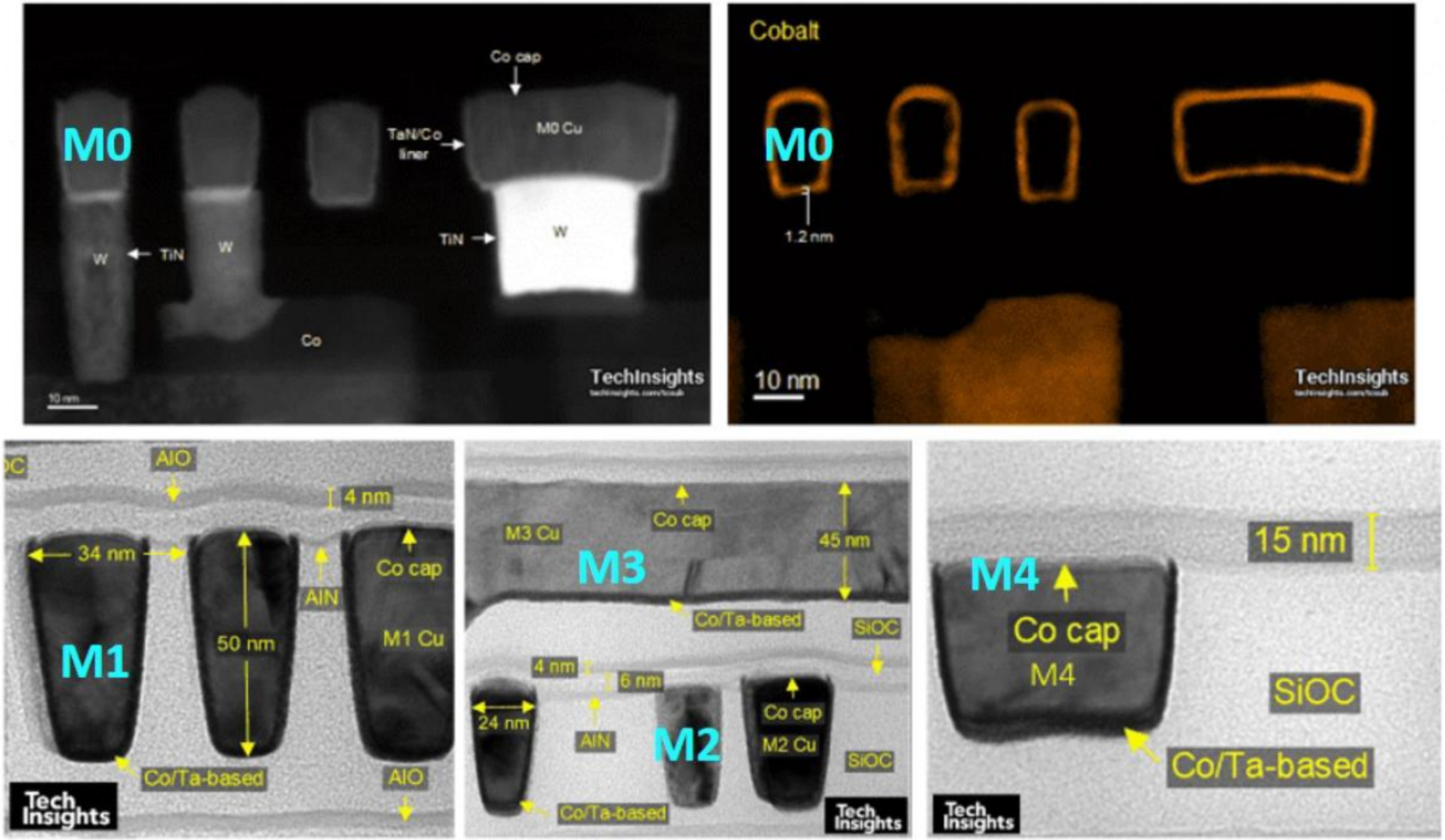


Sell (Intel) et al., VLSI 2022

Semiconductor-digest: Intel 4 Process Drops Cobalt Interconnect, goes with Tried and Tested Copper with Cobalt Liner/Cap

Cobalt (3): TSMC 5nm, Co liner and cap

Semiconductor-digest: Intel 4 Process Drops Cobalt Interconnect, goes with Tried and Tested Copper with Cobalt Liner/Cap



Co liner has been used in TSMC from 20 nm node

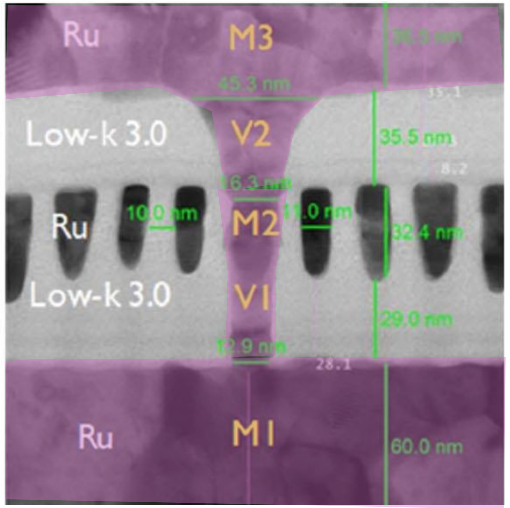
Courtesy of Techinsights

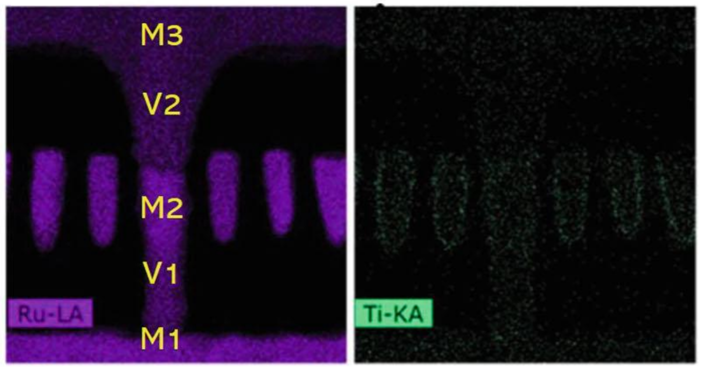
Yuan Tu,
AtomSolve Corp.

Ruthenium (1): IMEC 3nm & 2nm

3 nm

- **Dual-damascene**
- Ru/TiN liner, SiCOH dielectric (k=3)
- M3-M1 high-aspect-ratio **Supervia**

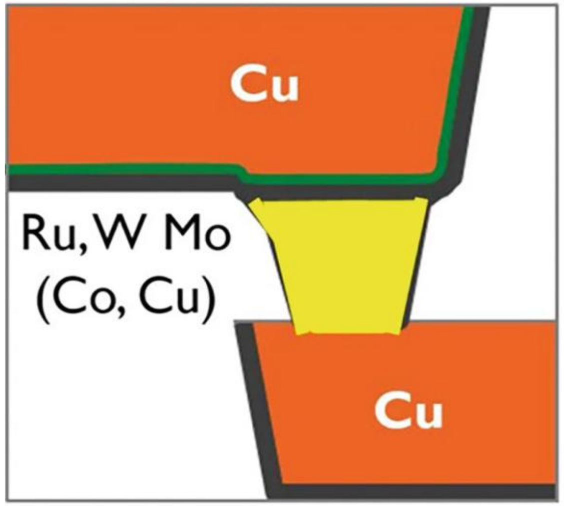


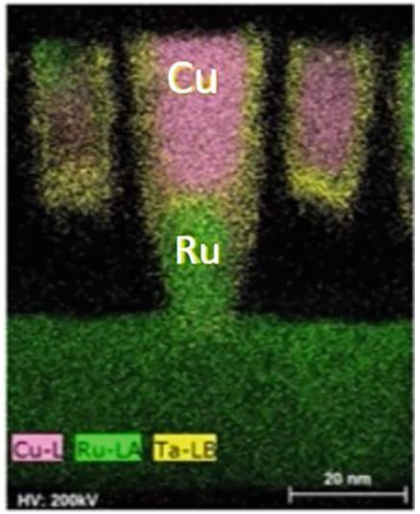


M1, M3 MP=36nm
M2, 21 nm

2 nm

- Hybrid metallization = **Single-damascene**
- M2 Cu/Ta, V1 Ru via with no Liner.
- Balance between Resistance and Reliability





MP = 21nm

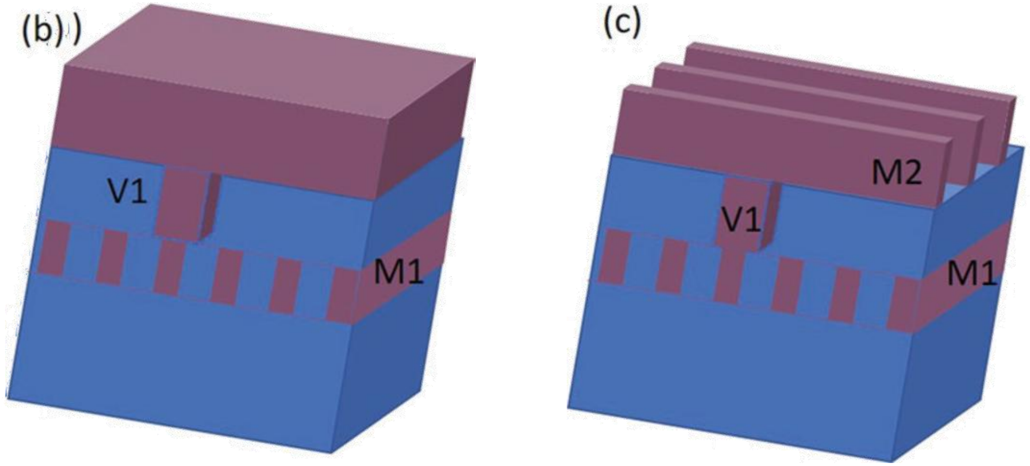
Yuan Tu,
AtomSolve Corp.

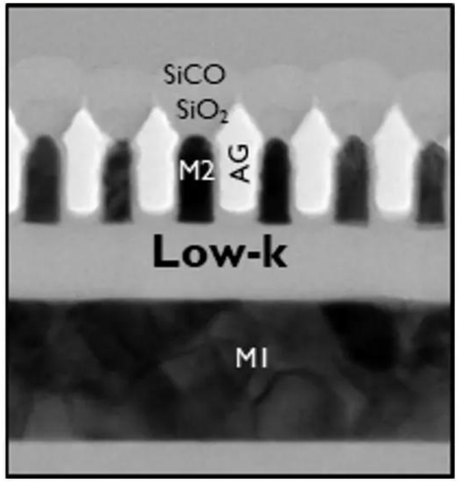
Ruthenium (2): IMEC 1.5nm Semi-damascene

MP<=21nm

- Via fill and overfill
→ Single-damascene

- M2 etch back
→ Semi-damascene

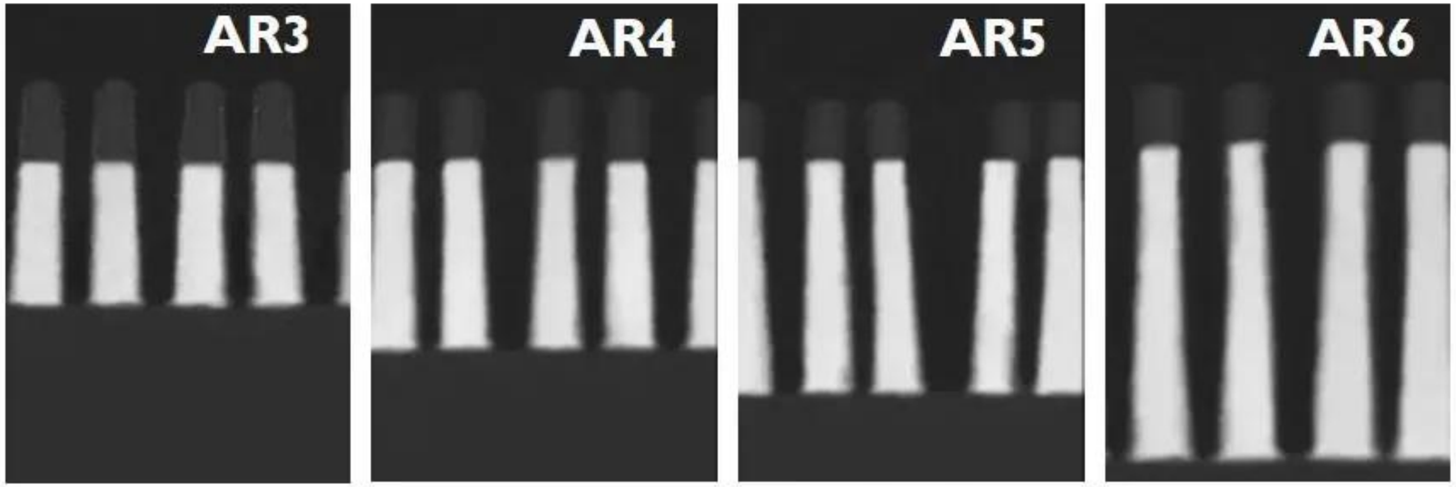




IMEC: A view on the logic technology roadmap (2020)

- Aspect Ratio (AR) ↑
→ Resistivity ↓

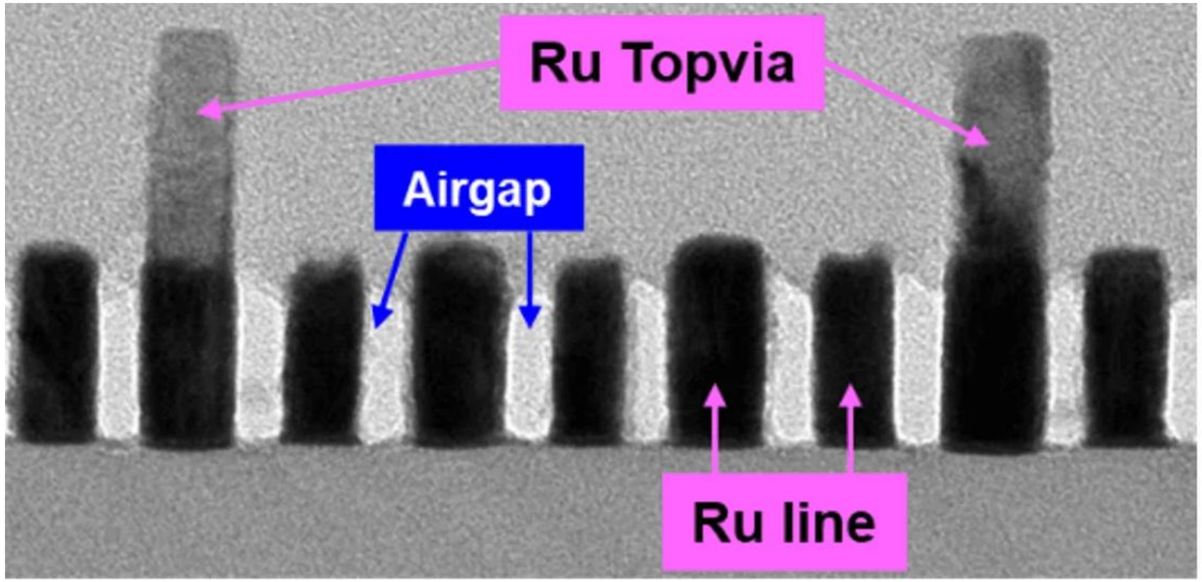
- Air gap (Low-k)
→ Capacitance ↓



IMEC: Semi-damascene metallization: inflection point in back-end-of-line processing? (2024)

Ruthenium (3): Ru + airgap

IBM: Subtractive Ru TopVia

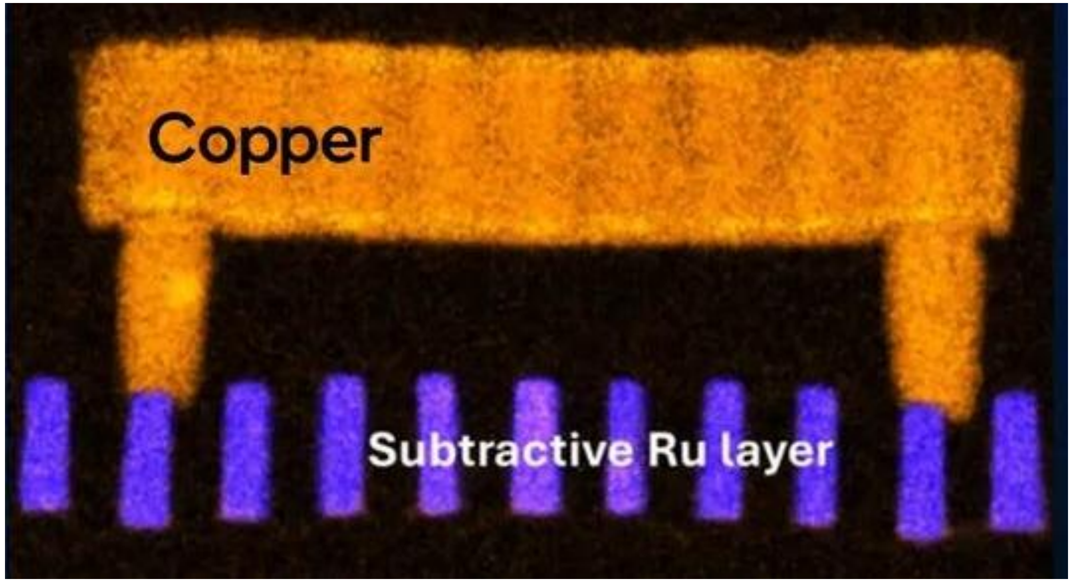


Address via-to-line alignment problem.

The metal line is trimmed by a sidewall spacer and the via is located by the same spacer stack. SALELE litho.

https://research.ibm.com/blog/beol-cu-interconnects-iedm

Intel: Subtractive Ru

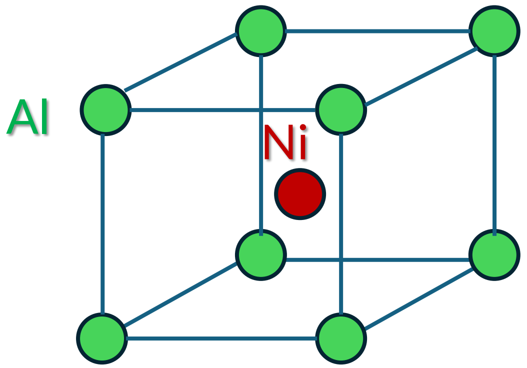


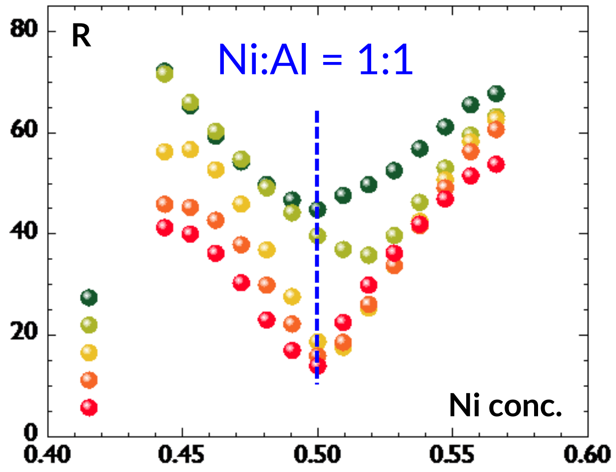
Cost-efficient for HVM subtractive Ru integrated process
No airgap exclusion zones around vias,
No self-aligned via flows that require selective etches.

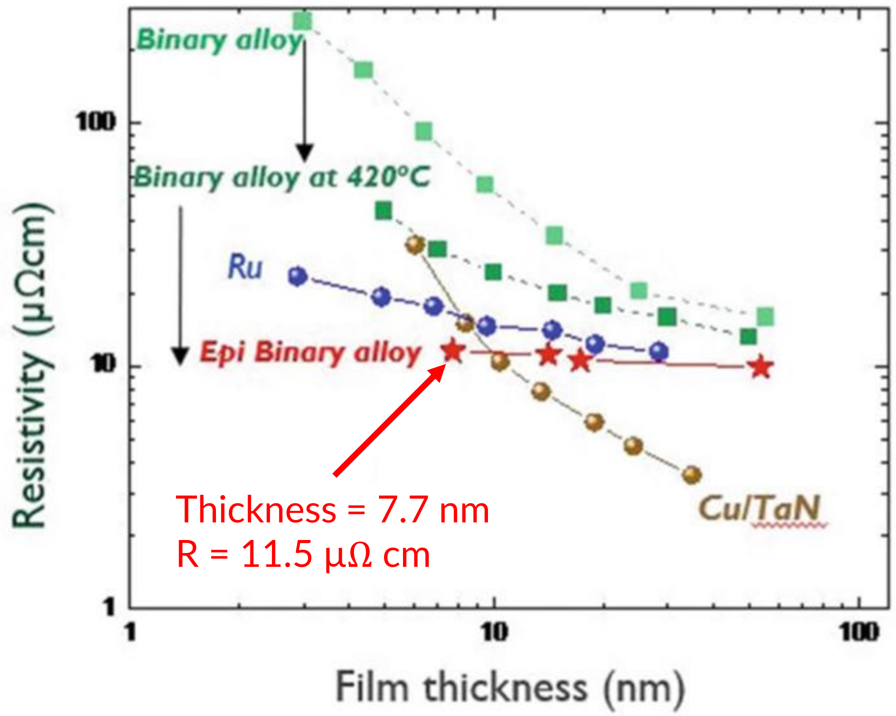
IEDM 2024: Intel Foundry Unveils Breakthroughs in Interconnect Scaling for Future Nodes

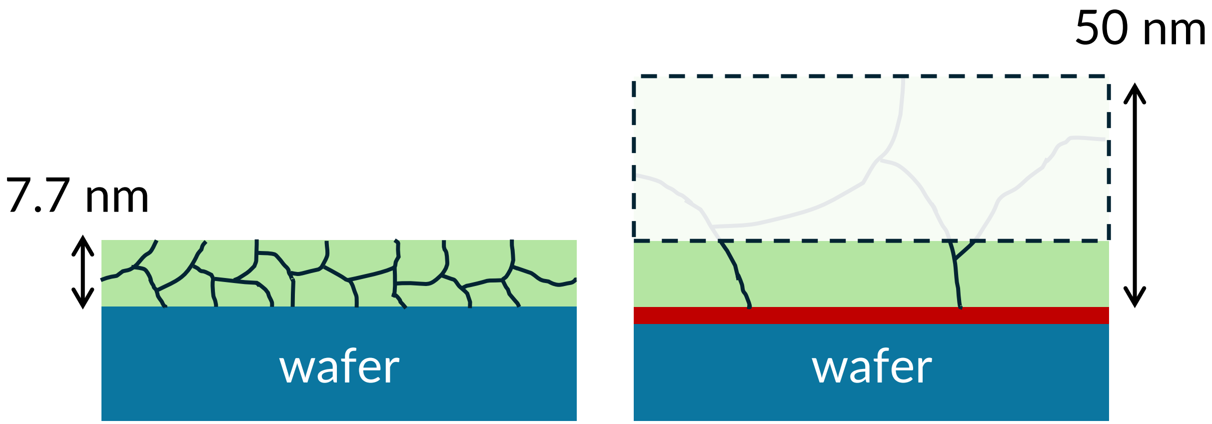
Intermetallic compounds: NiAl

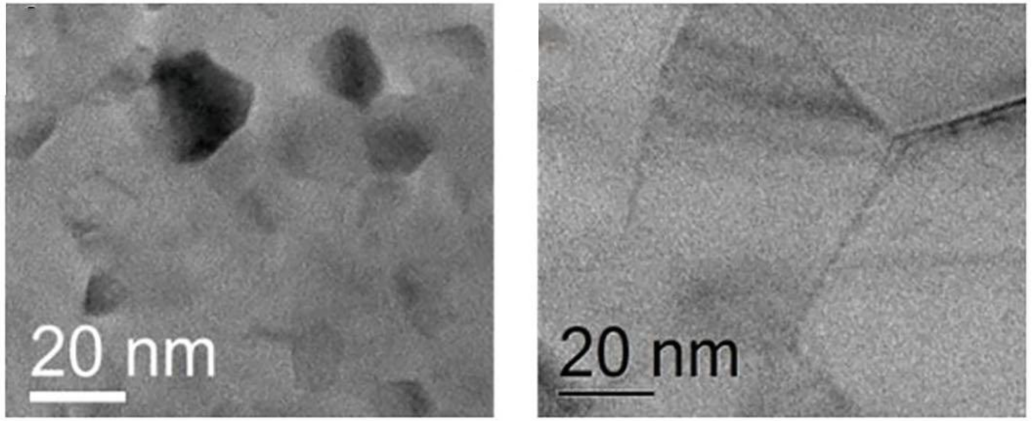
Ref: [1] Soulié et al., IEEE IITC 2020 (imec)
[2] Conductor films with lower resistivity than Cu and Ru (imec)



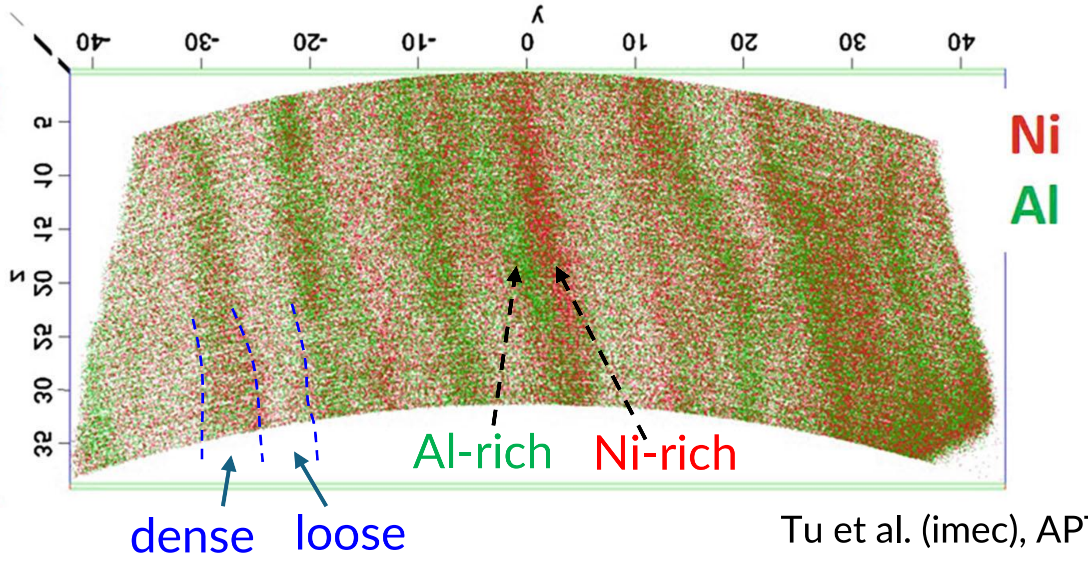








Non-uniformity of NiAl

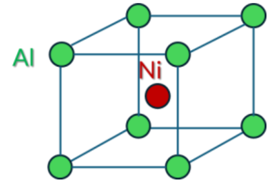


NiAl resistivity still higher than theoretical value

Reason: Distribution in NiAl is not uniform?

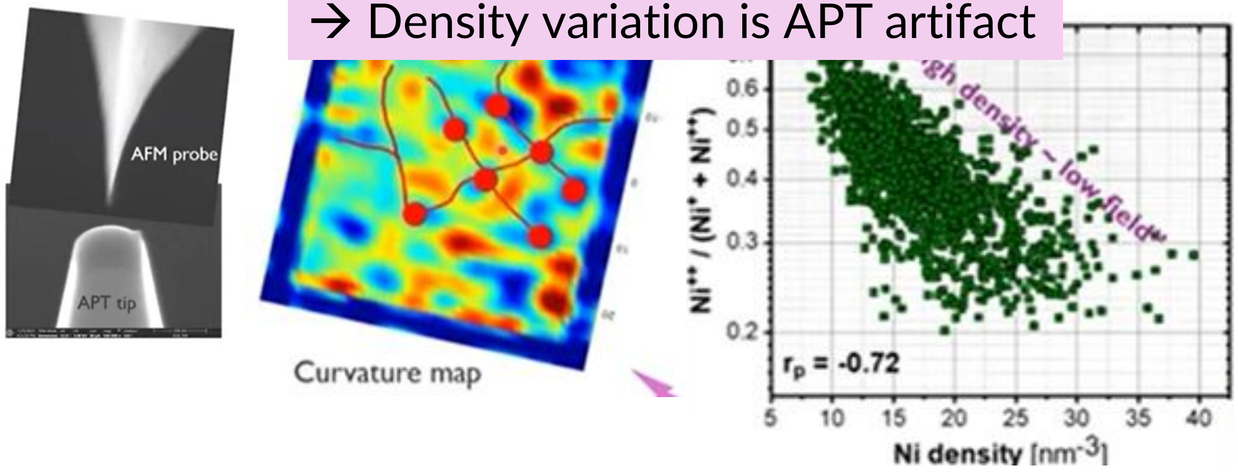
← Atom Probe Tomography (APT) results:

1. Atomic density: dense and loose regions
2. Ni and Al conc. fluctuations (not 1:1)



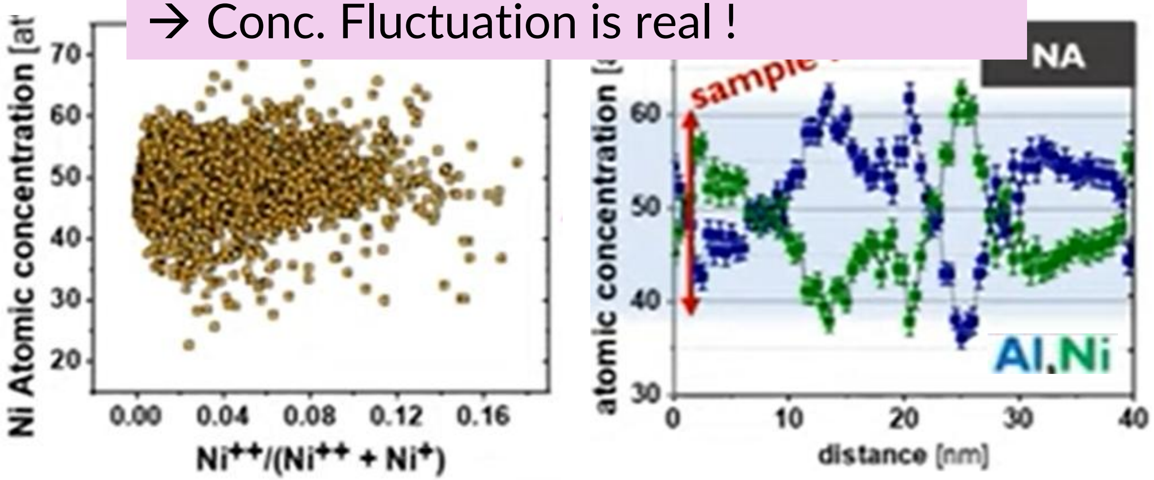
Tu et al. (imec), APT & M 2022

Density ~ Curvature ~ Field
→ Density variation is APT artifact



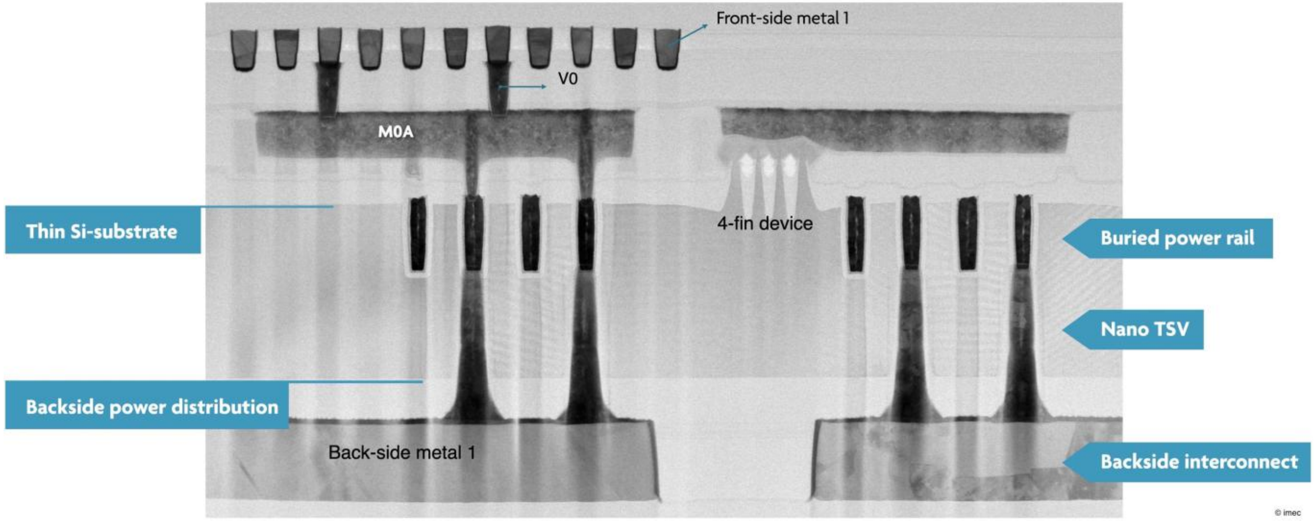
Tu et al. (imec), APT & M 2022

Conc. is irrelevant to field
→ Conc. Fluctuation is real !

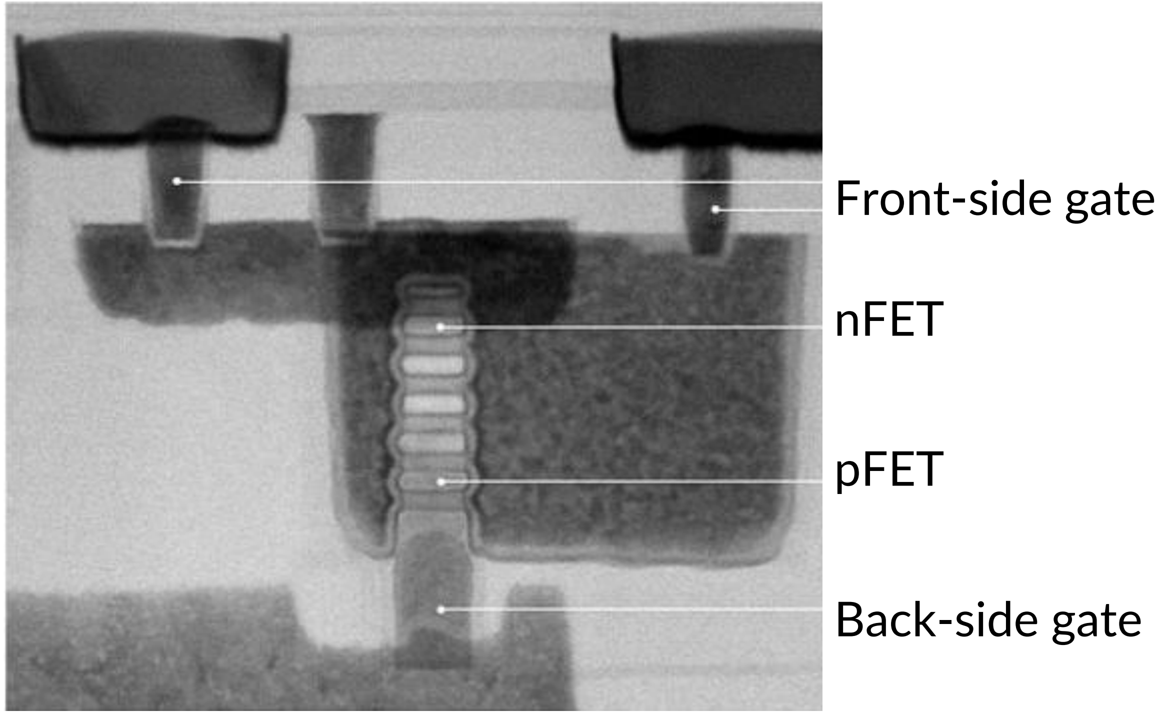


Jeroen et al. (imec), APT & M 2022

Backside Power Delivery Network (BSPDN)



https://www.imec-int.com/en/articles/how-power-chips-backside

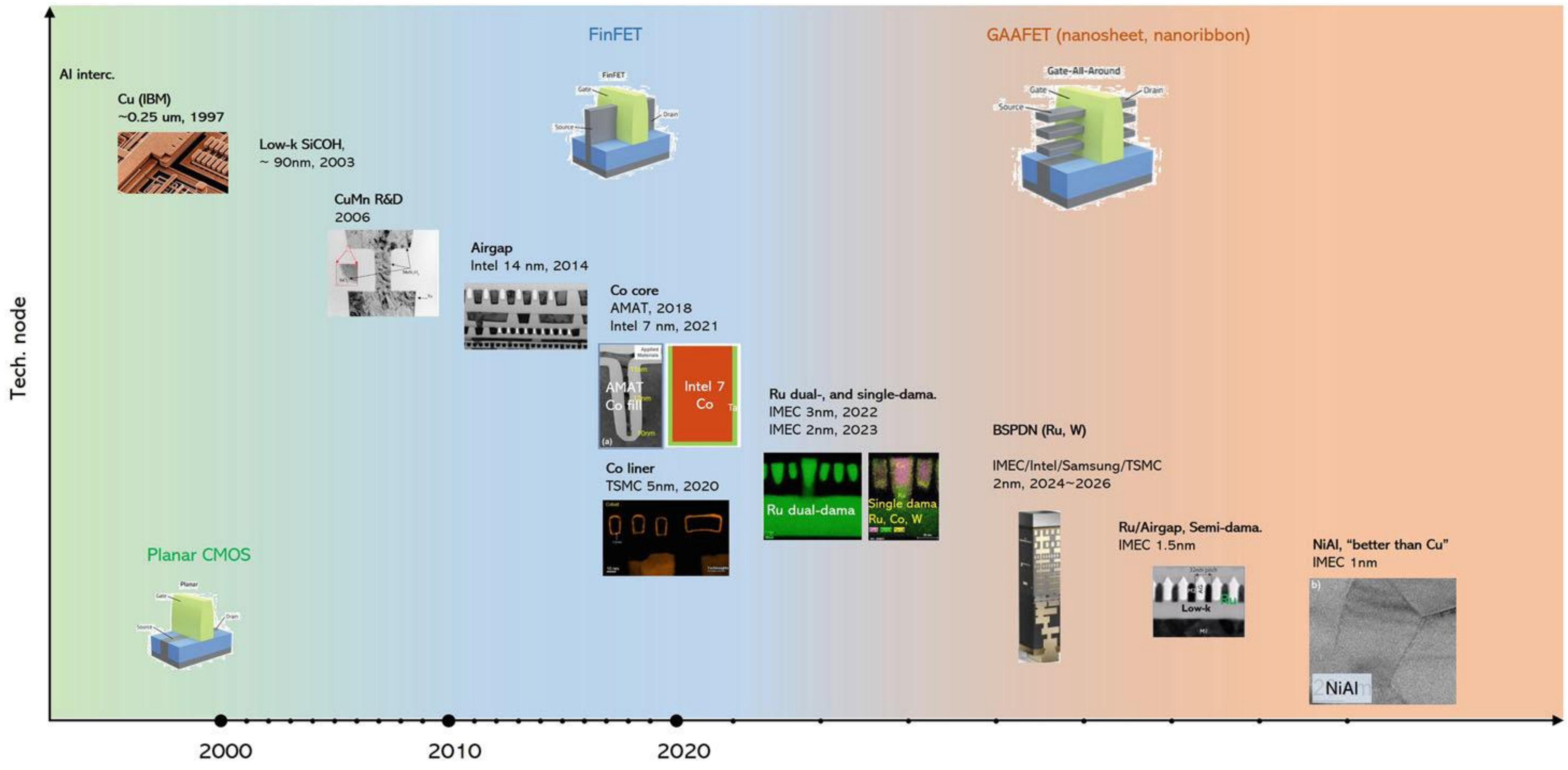


https://www.imec-int.com/en/events/imec-70th-international-electron-devices-meeting-iedm

Except for Materials, Architectures innovation is needed.
BSPDN is blurring the boundary between BEOL and Advanced Packaging

Summary

- Interconnect materials innovation is also driving force of Moore's law.



Yuan Tu, Book: Insights into semiconductor technologies, Springer nature (2025)

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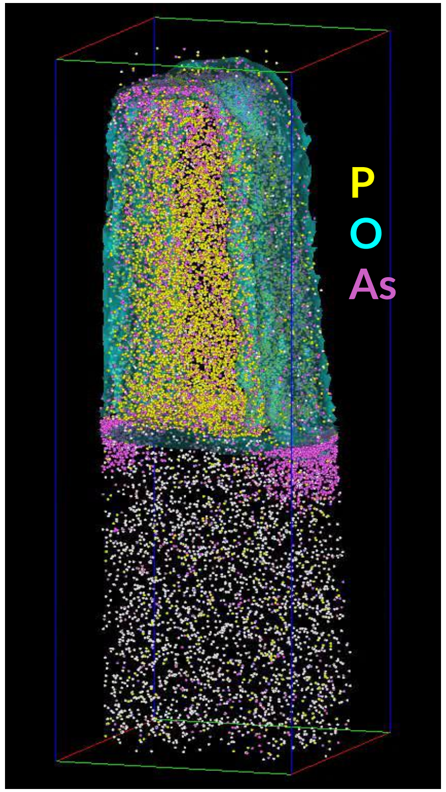
多尺度芯片解析、技術調研

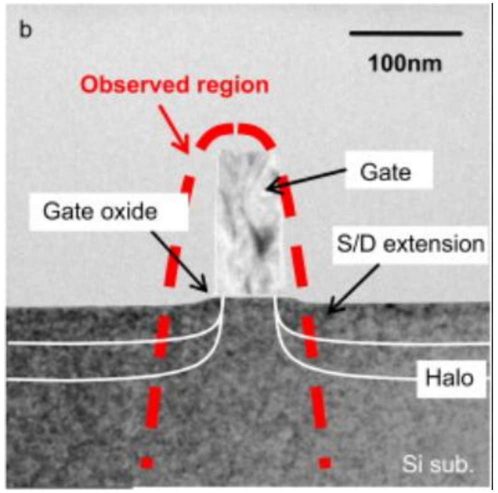
- 封裝級 um

Image: Binghamton Univ.

- 互連 nm→um
- 原子級 atomic



- 晶體管 nm



Inoue et al., Ultramicroscopy 109, 1479 (2009)